Communication for Computing

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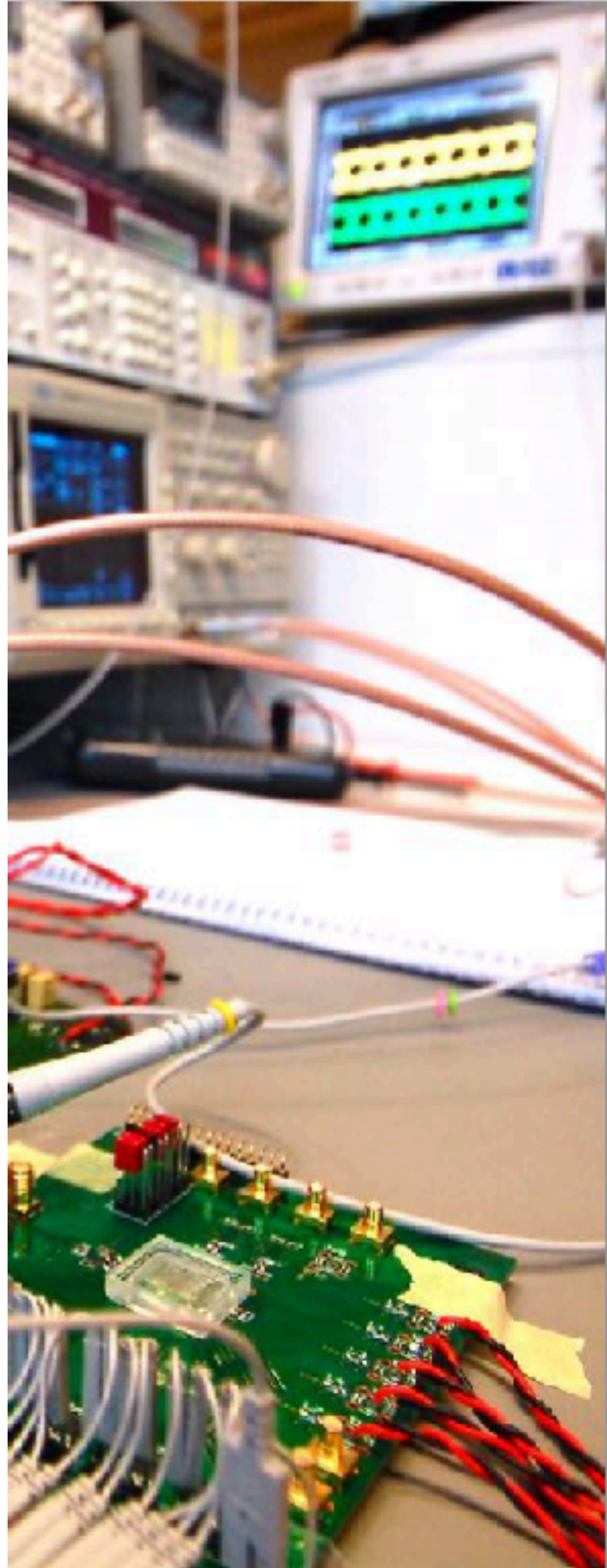
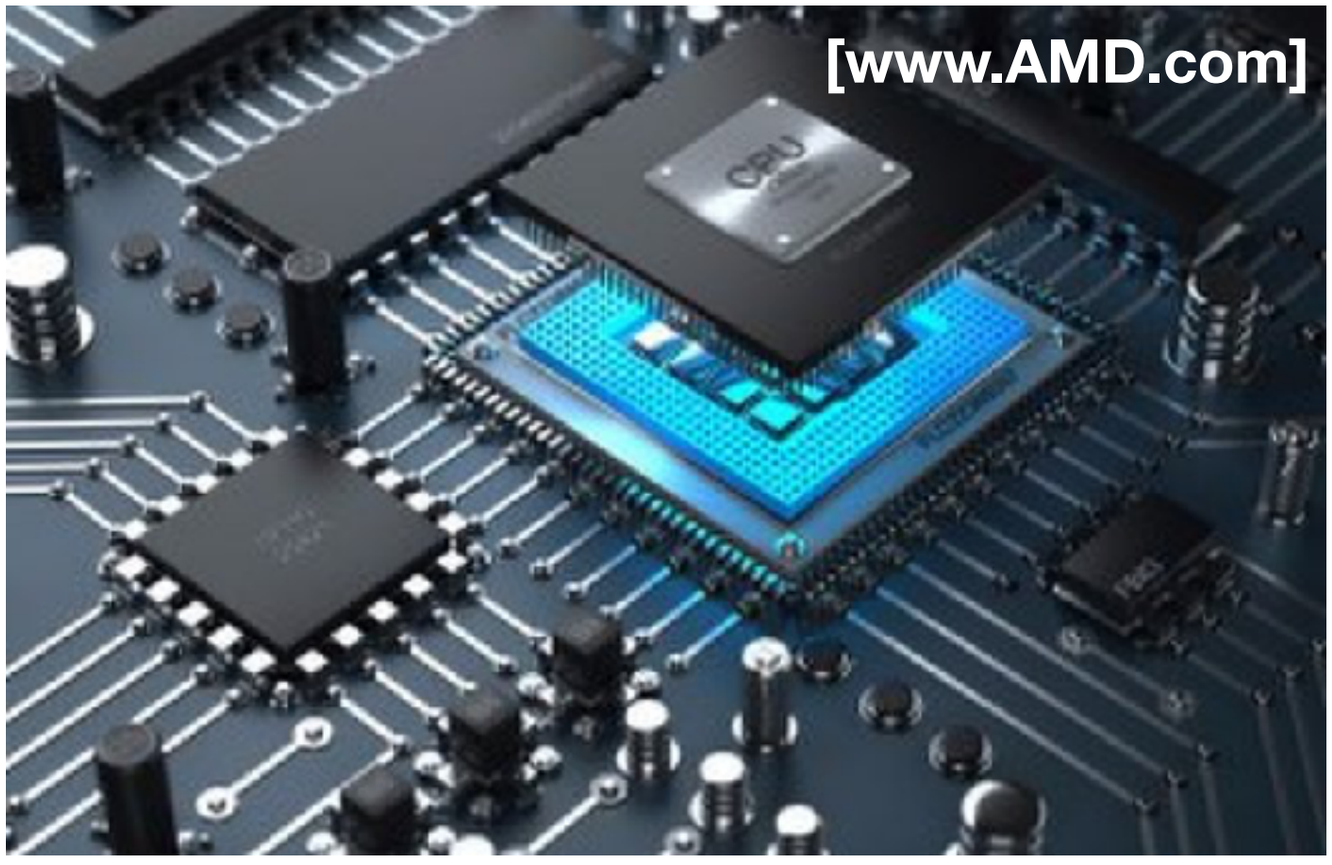
Outlook

- History of High-Performance Computing (HPC)
- Advanced Communications schemes for HPC
- Summary

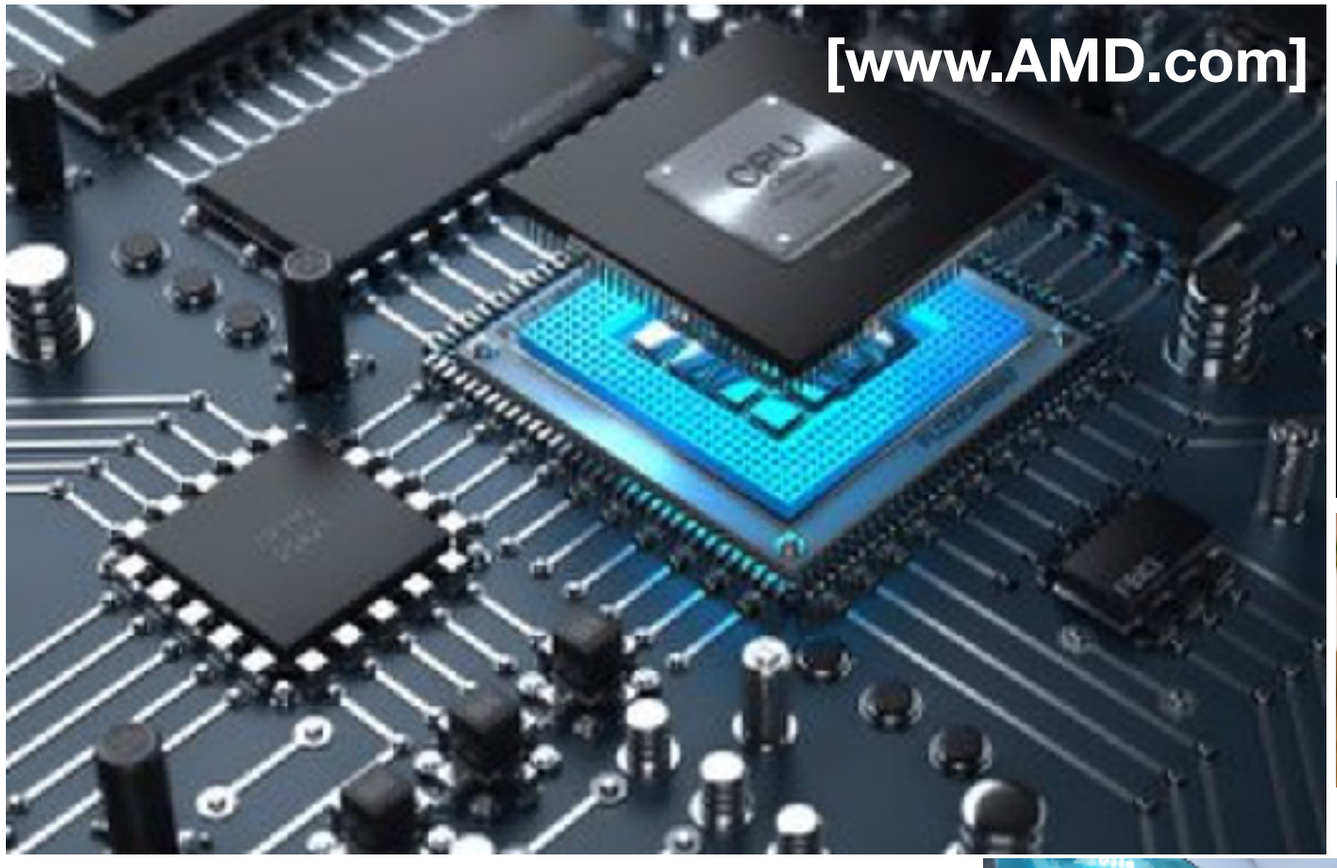
High-Performance Computing
History & Roadmap

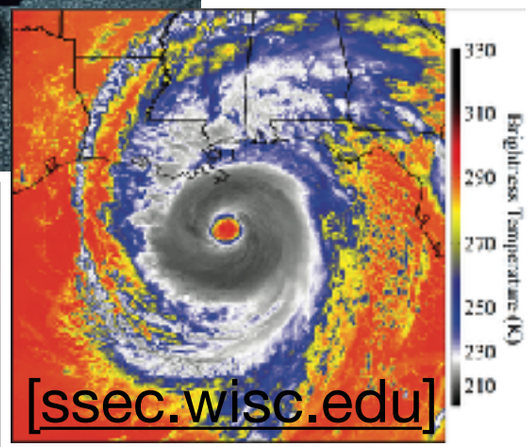


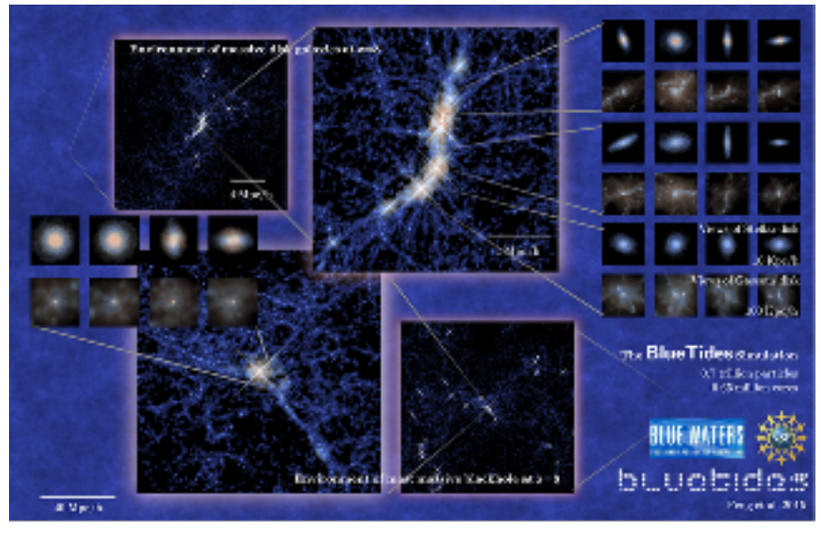
Modern Processor



Modern Processor







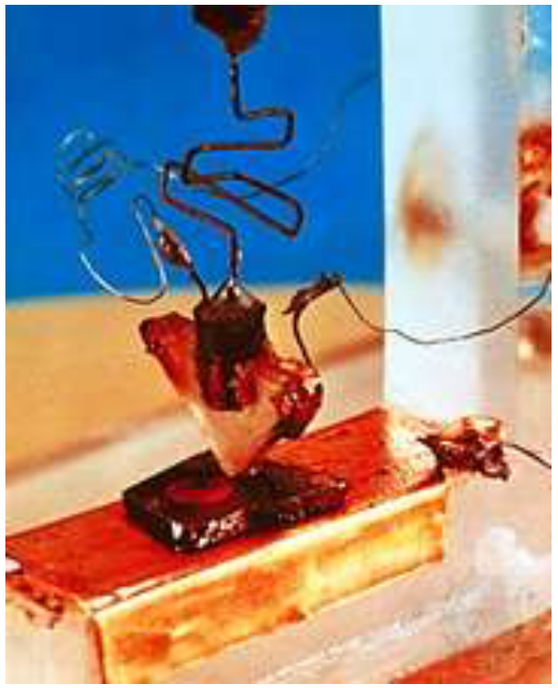
Bing

Modern Processor: History

Step 1: Transistors

- **Transistors** were invented to control the motion and the trajectory of the electrons to perform high-speed and complex ***Signal Processing Schemes***

- A transistor is a fundamental element that can be used to **map** a computational concept or an algorithm into reality.

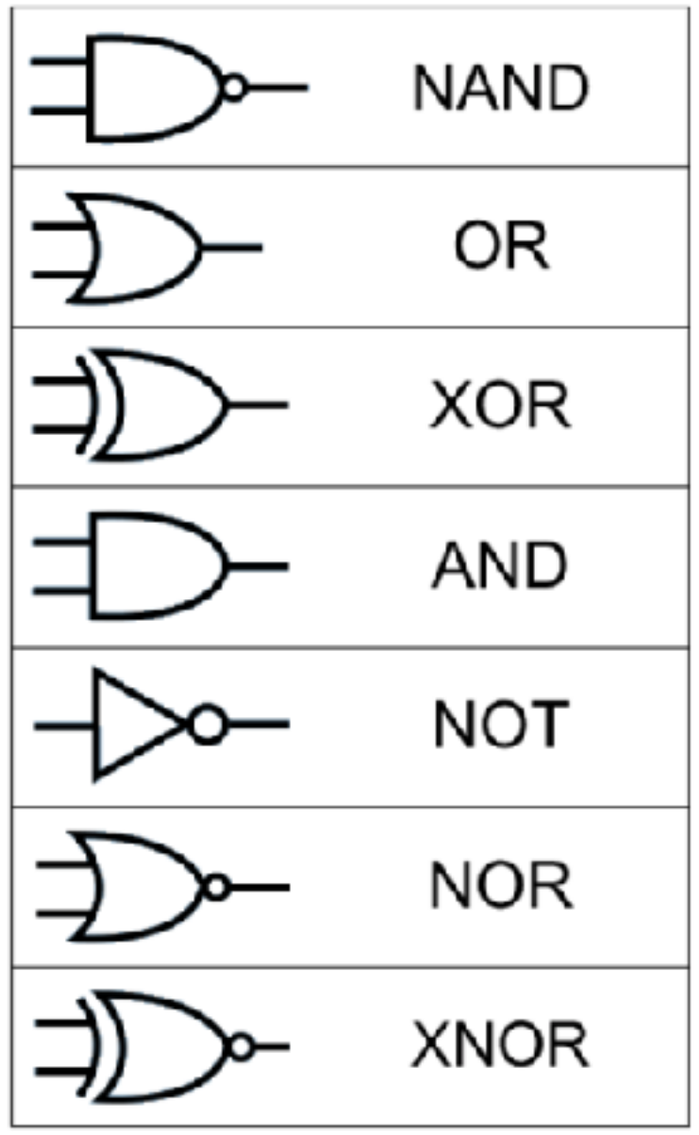


[ComputerHistroy.Org]

Modern Processor: History

Logic Operators

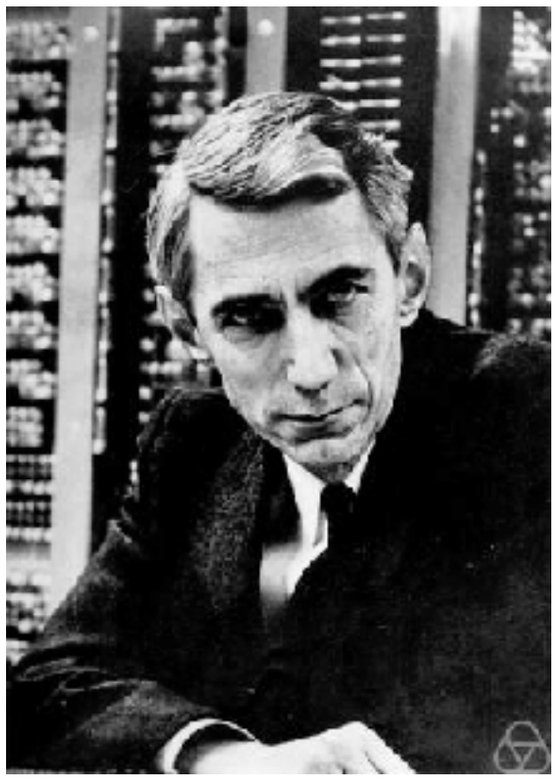
- Transistors are well suited to implement logic operators
- There are some specific topological arrangement of transistors that can be used to implement the logic operators



Modern Processor: History

Digital Circuit Design Theory

- 1937: Master Thesis (MIT)
- **Title:** A symbolic analysis of relay and switching circuits
- Used the binary properties of the electronic circuits and switches to perform logic operation using Boolean algebra.

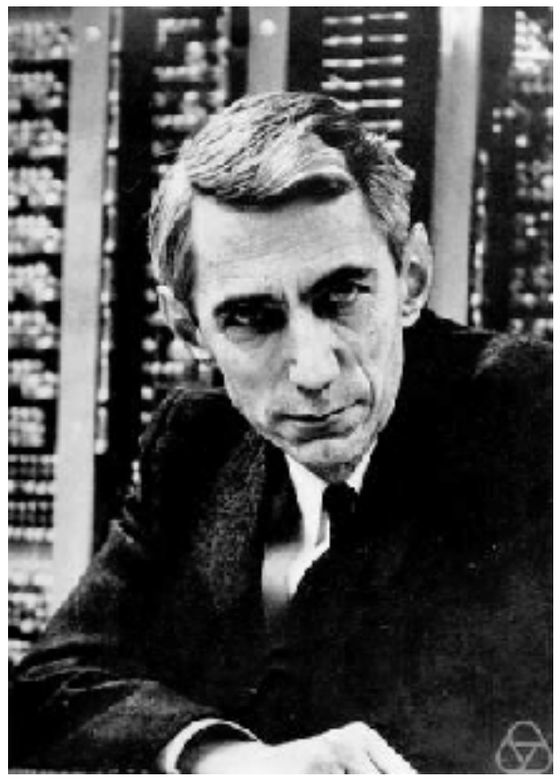


[wikipedia.Org]

Modern Processor: History

Step 2: Information Theory

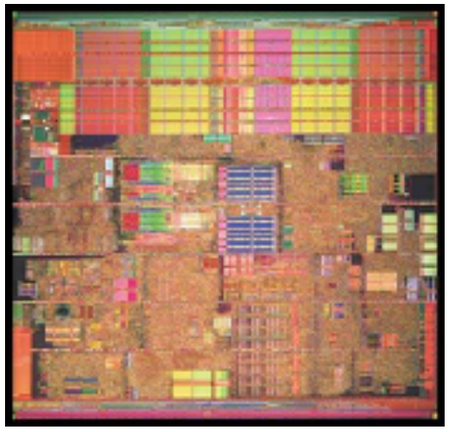
- Realizing logic circuits for **Computing**
- A Mathematical Theory of **Communications** (1948)
- Probably this was the first time that people noticed the duality of **the Communication and the Computation**

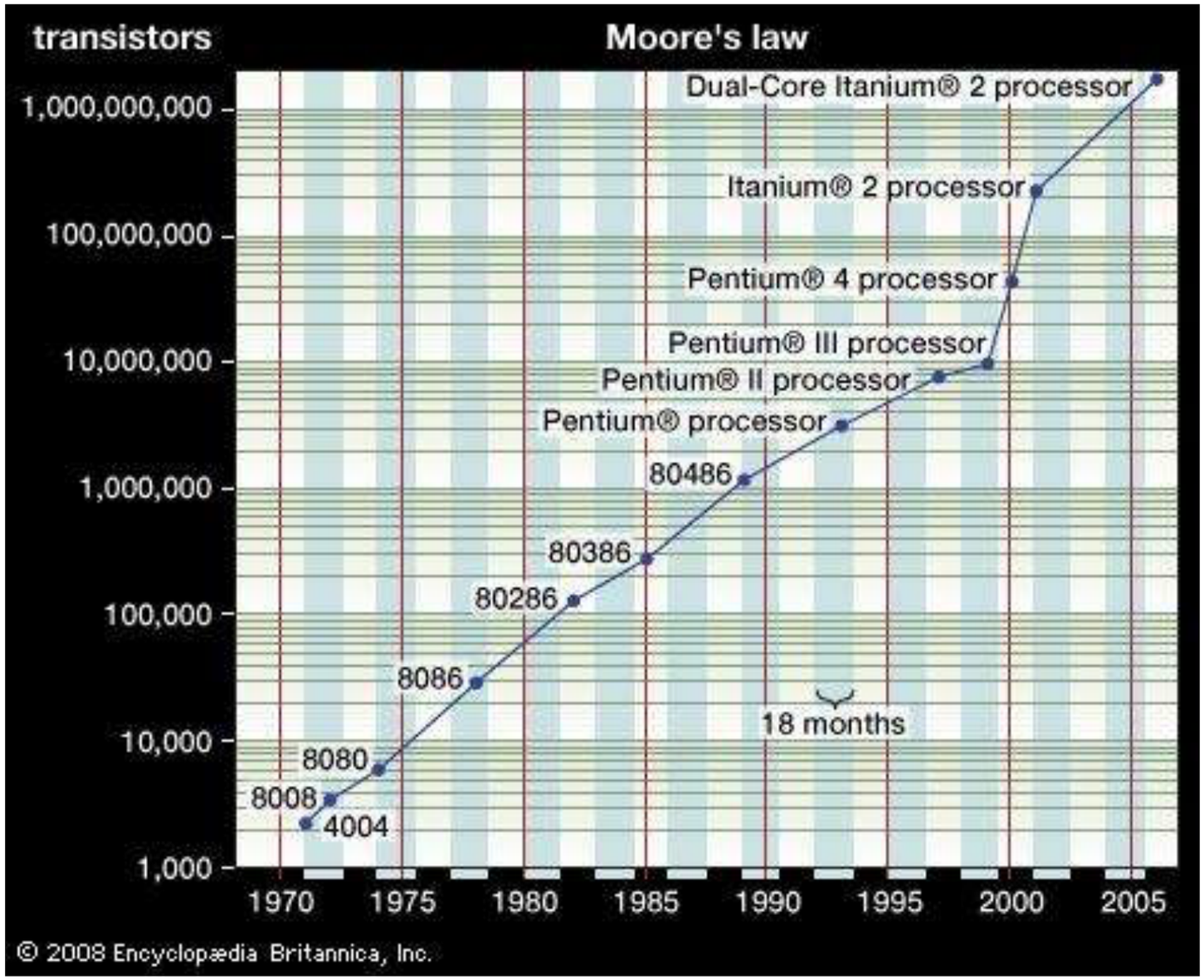


[wikipedia.Org]

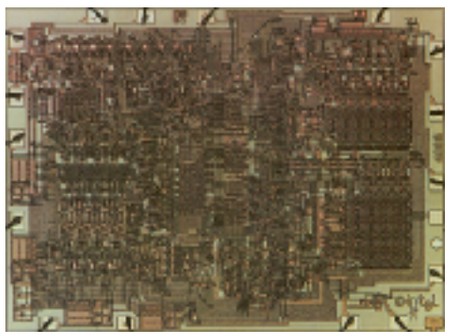
Modern Processor: CMOS Processors

Intel Pentium 4





Intel 4040

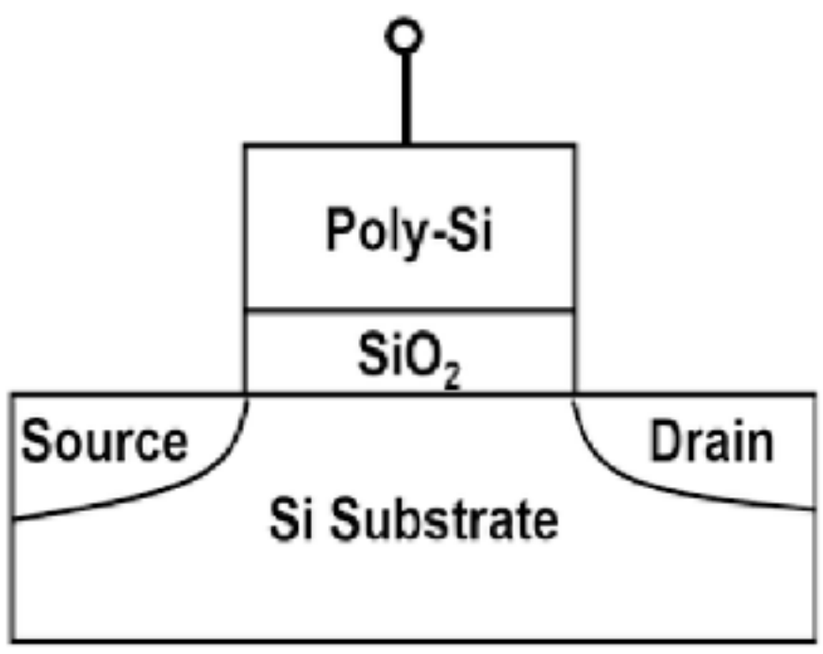


[intel.Com]

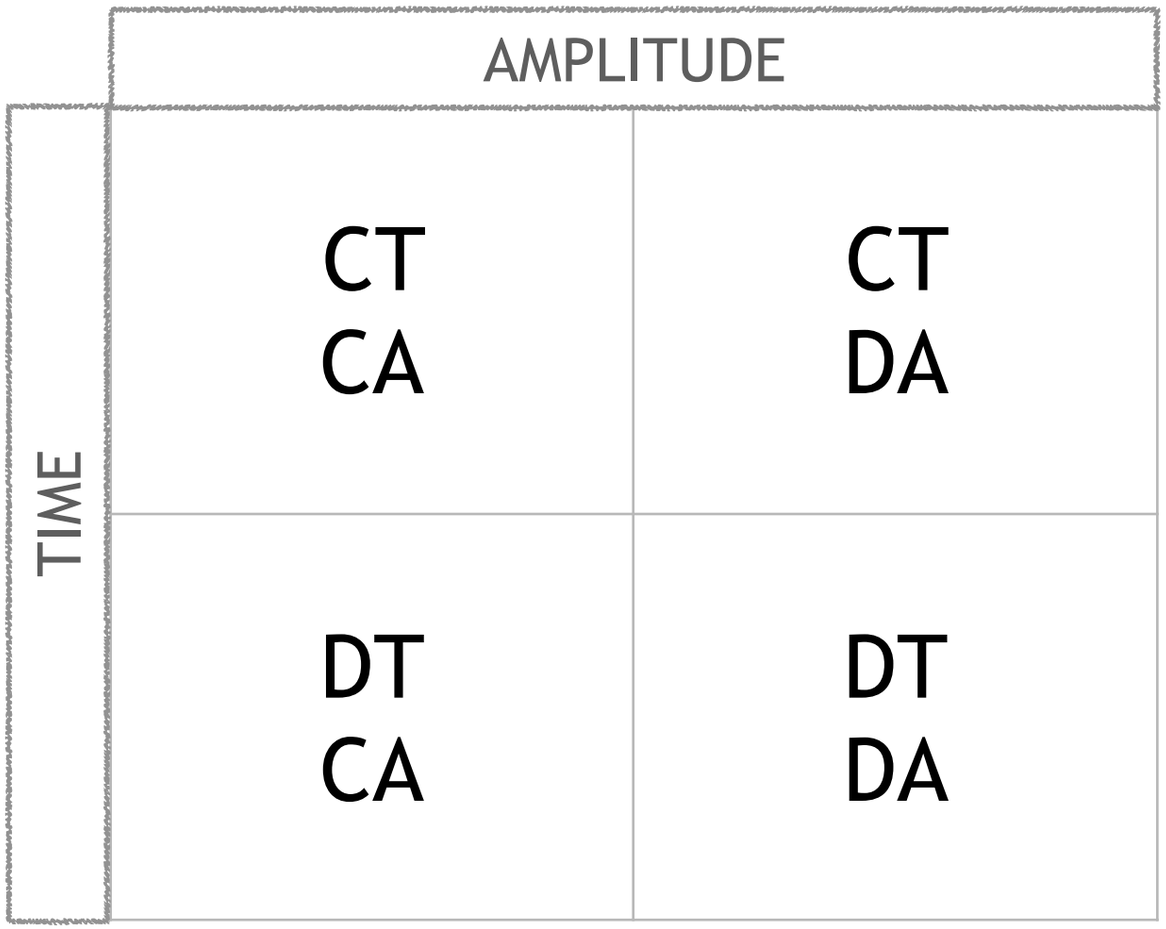
Modern Processor: Fundamental Building Block

- **Switch/non-linear** physical element to implement logic operators
- **Linear** to implement amplifiers
- Able to do **discrete-time signal processing** and **continuous-time signal processing**, both.

- **In summary:** a MOS device is the fundamental building block for mapping signal processing schemes into hardware.

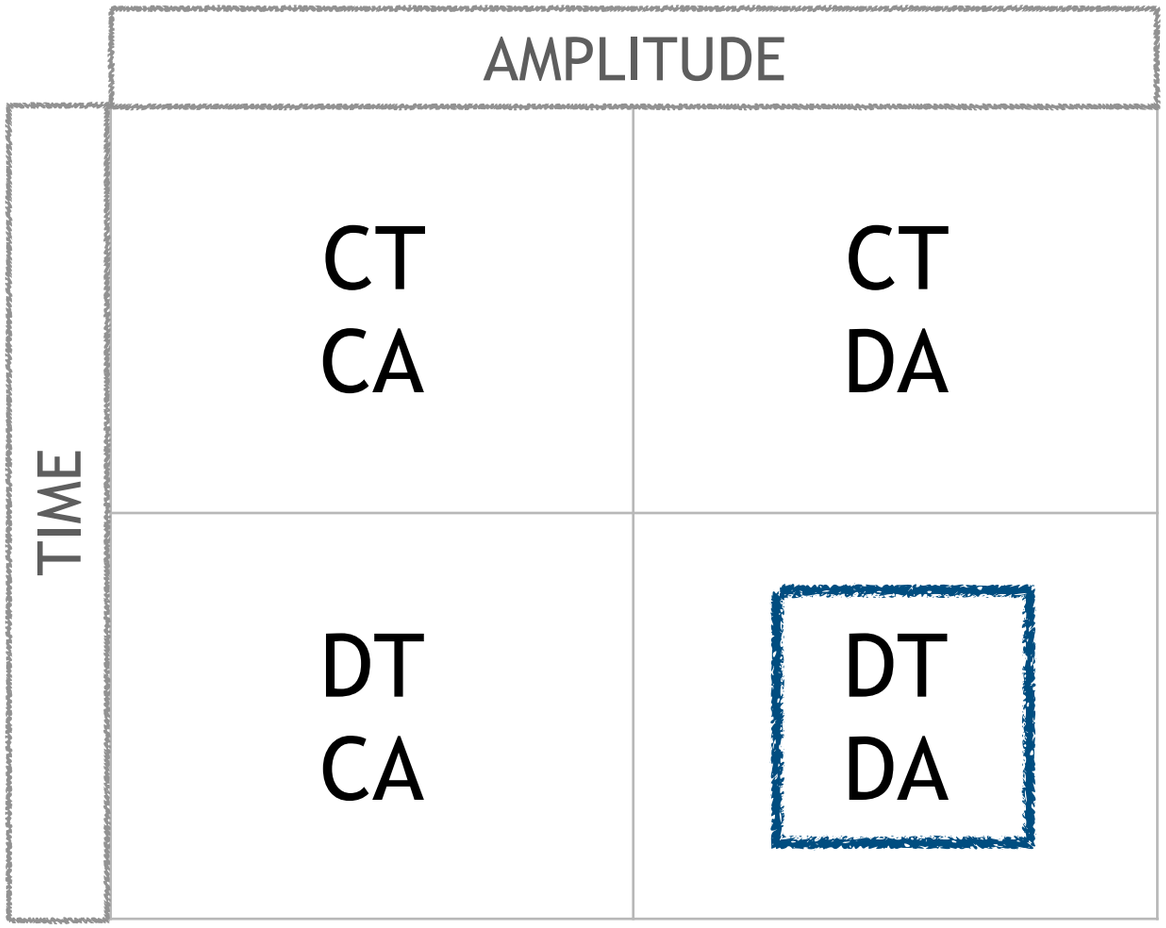


Modern Processor: Signal Processing



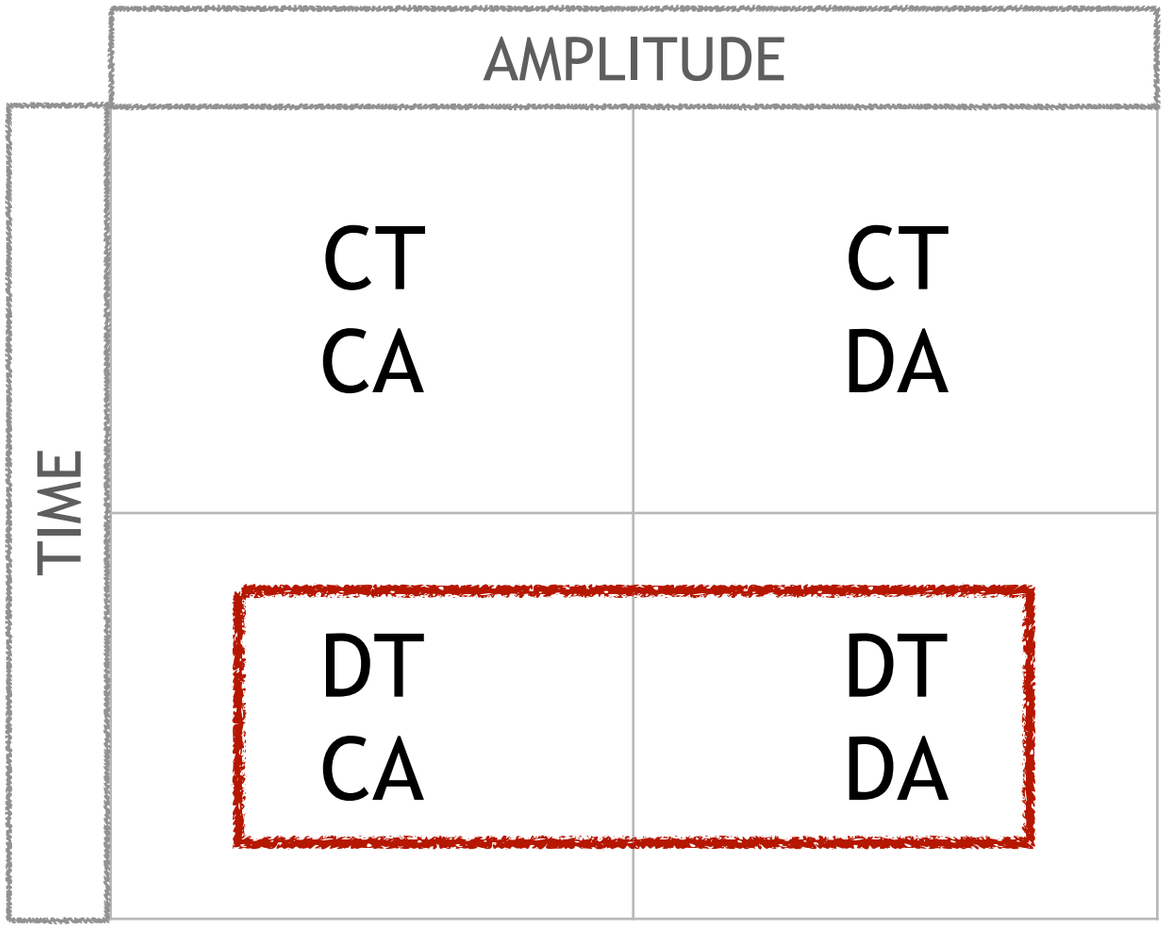
CT: Continuous-Time
DT: Discrete-Time
CA: Continuous-Amplitude
DA: Discrete-Amplitude

Modern Processor: Signal Processing



Digital Signal Processing

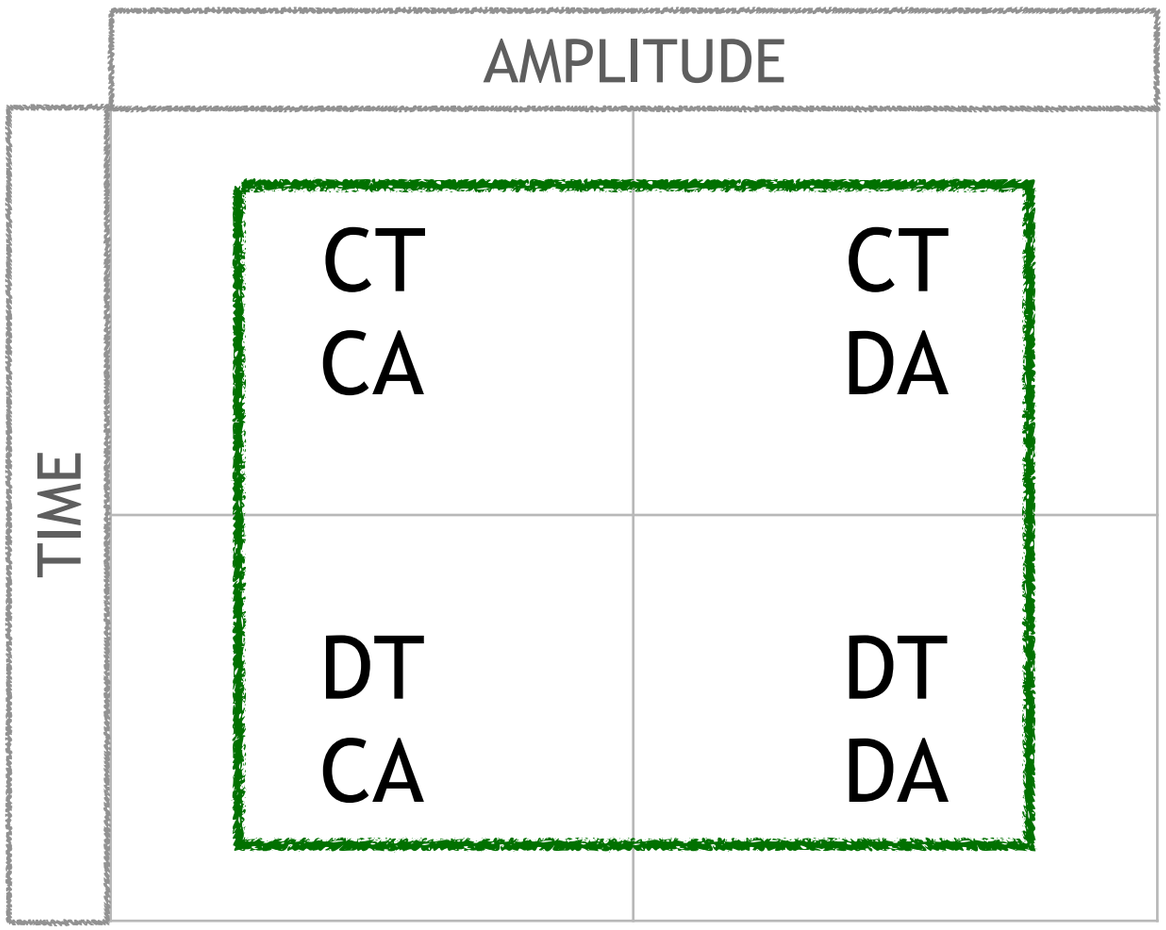
Modern Processor: Signal Processing



DSP: Discrete-Time Signal Processing

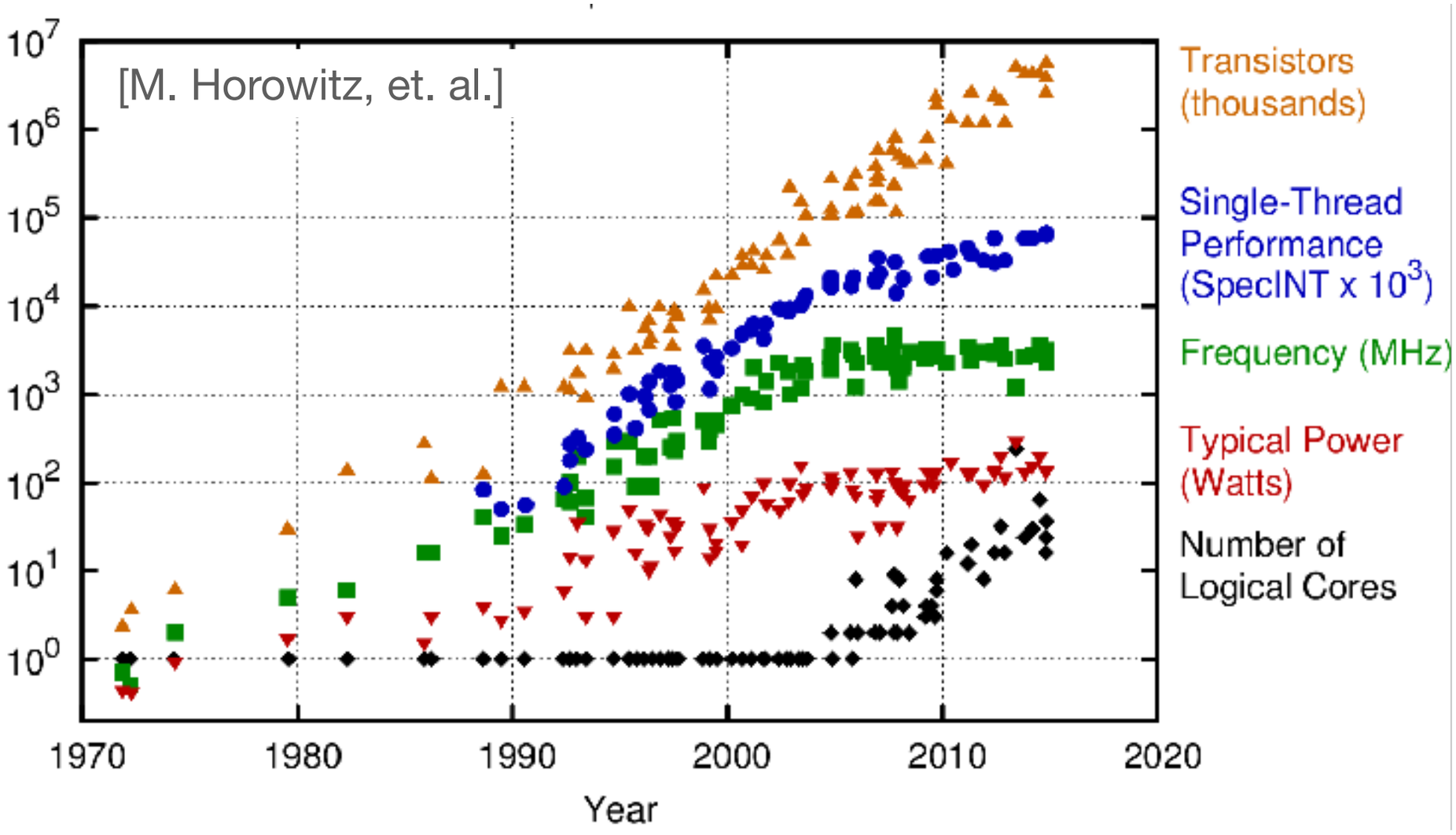
Based on Shannon-Nyquist Sampling Theorem

Modern Processor: Signal Processing



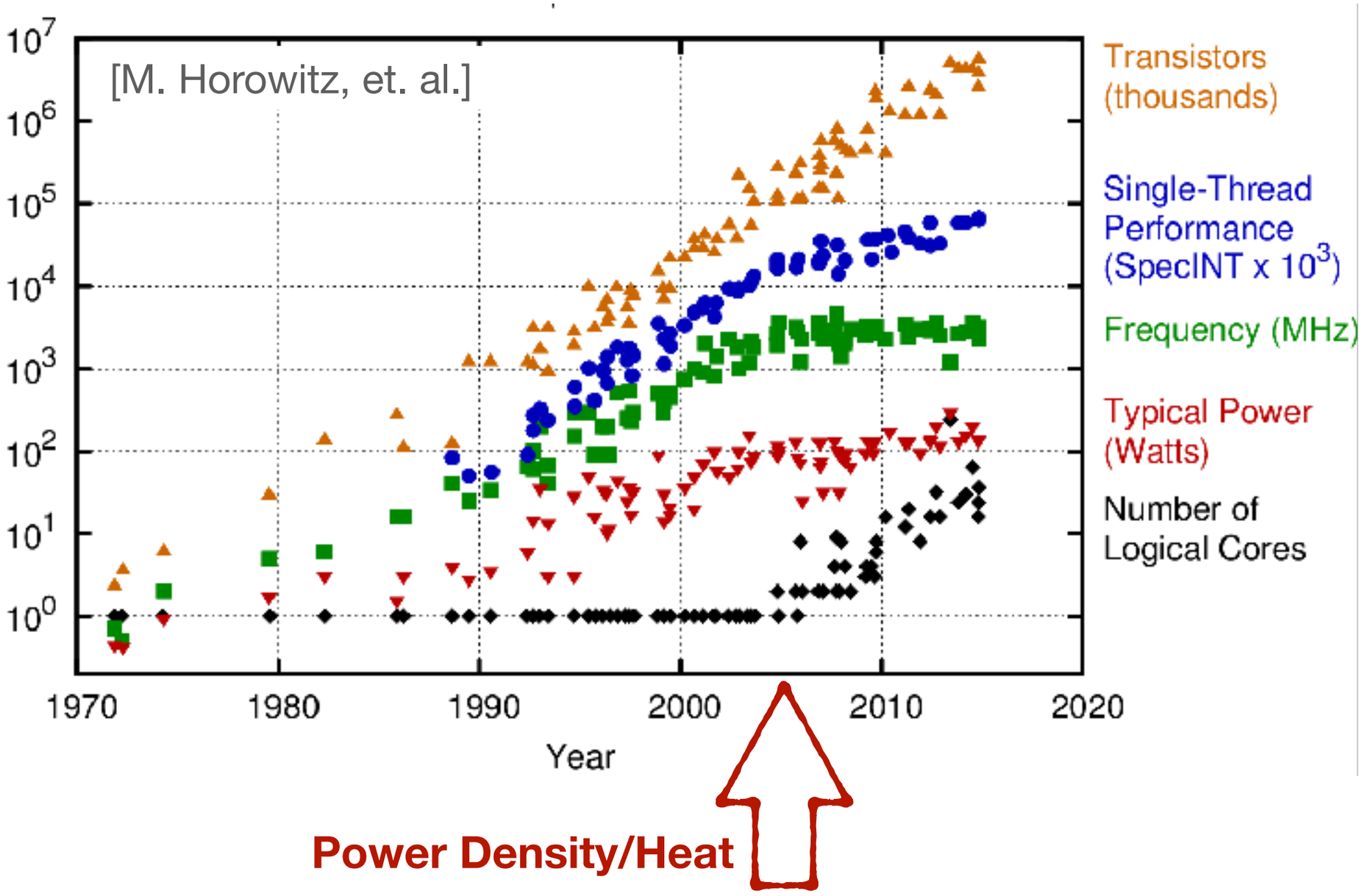
ASP: Analog Signal Processing

Processing Power: Trend



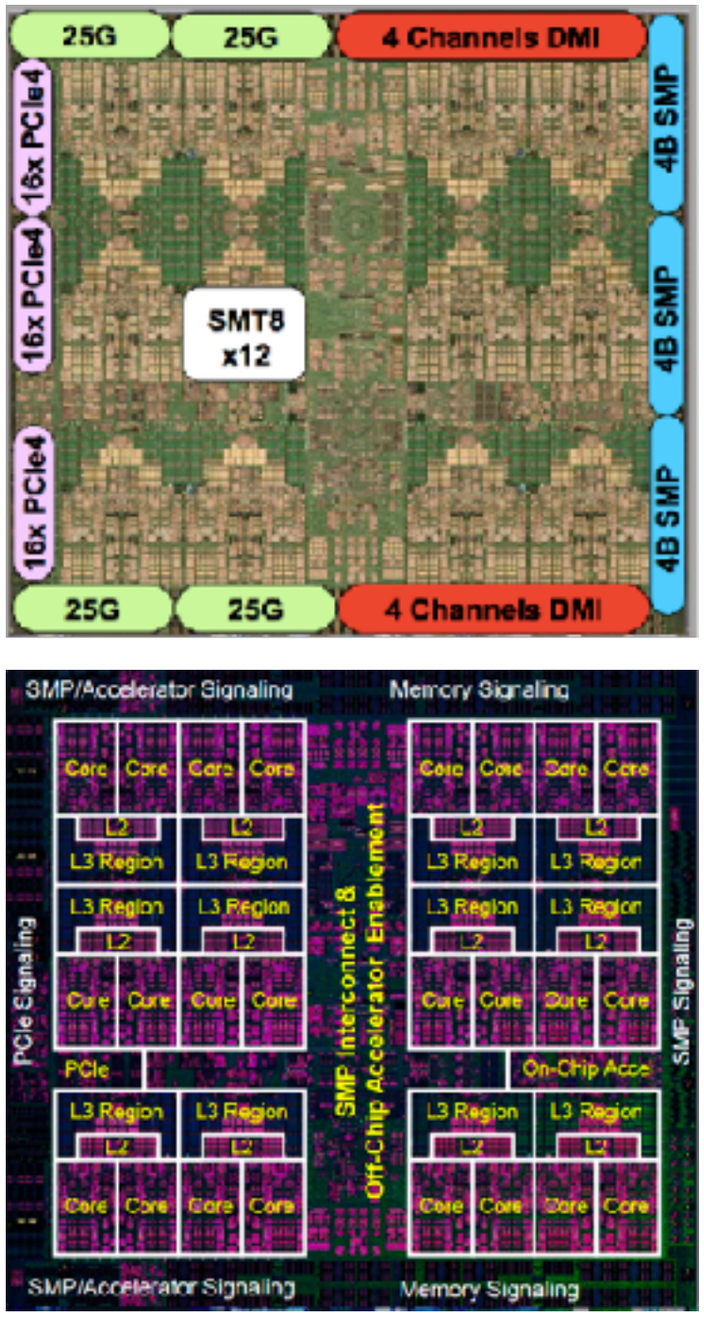
[M. Horowitz, et. al.]
[karlrupp.net]

Processing Power: Power Density and Heat



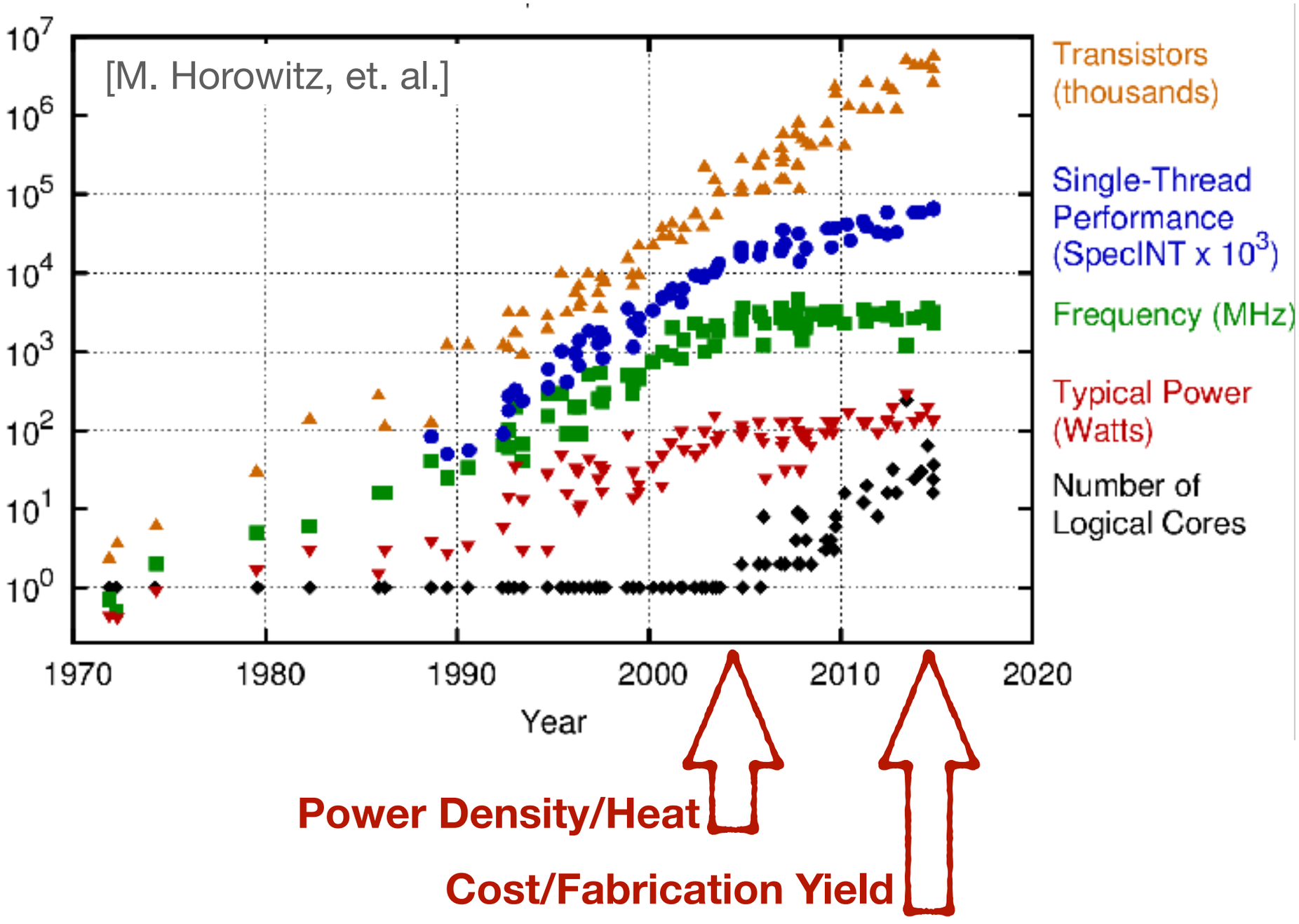
Processing Power: Power Density and Heat

- **Solution: Multi-Core Processor**
  - IBM Power9
  - 24x cores
  - 14 nm FinFET, 17 ML, 8B transistors
  - Includes eDRAM and SRAM
  - 16 and 25 Gb/s interfaces
  - 13 Tb/s off chip BW
  - Power consumption (approximately):
    - Core: 57%
    - Clock: 10%
    - Cache: 5%
    - I/O: 15%
    - Leakage: 13%

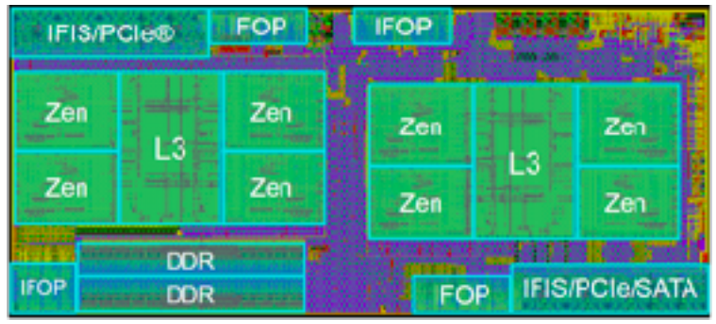


[IBM, ISSCC'2017]

Processing Power: Yield and Cost

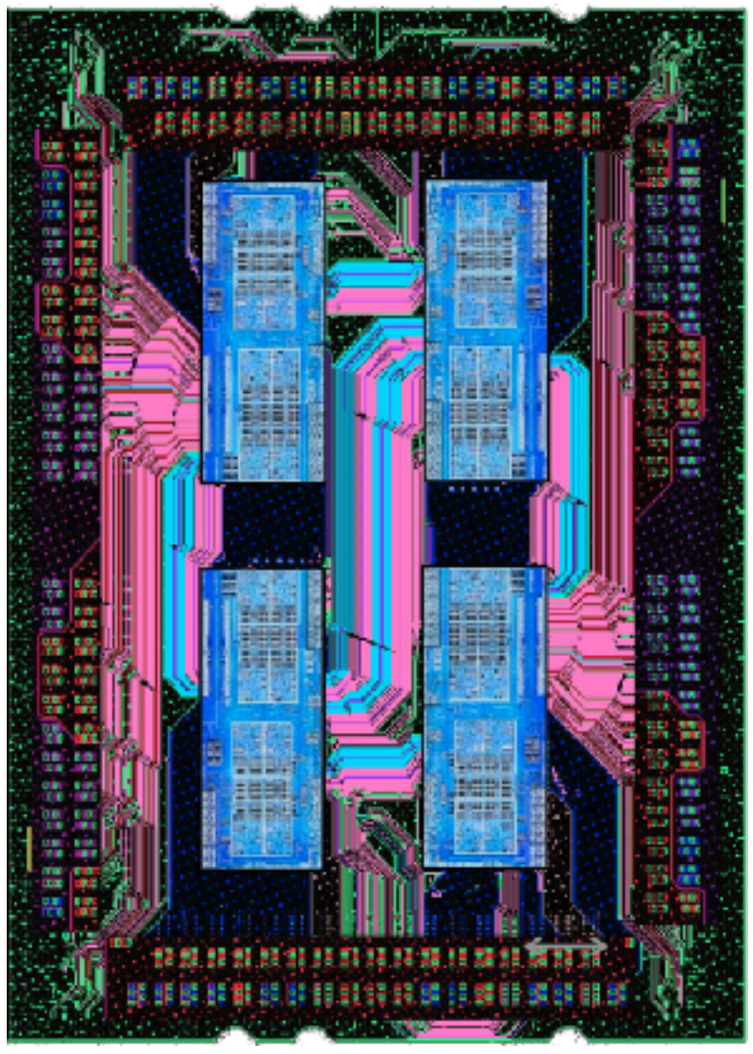


Processing Power: Yield and Cost



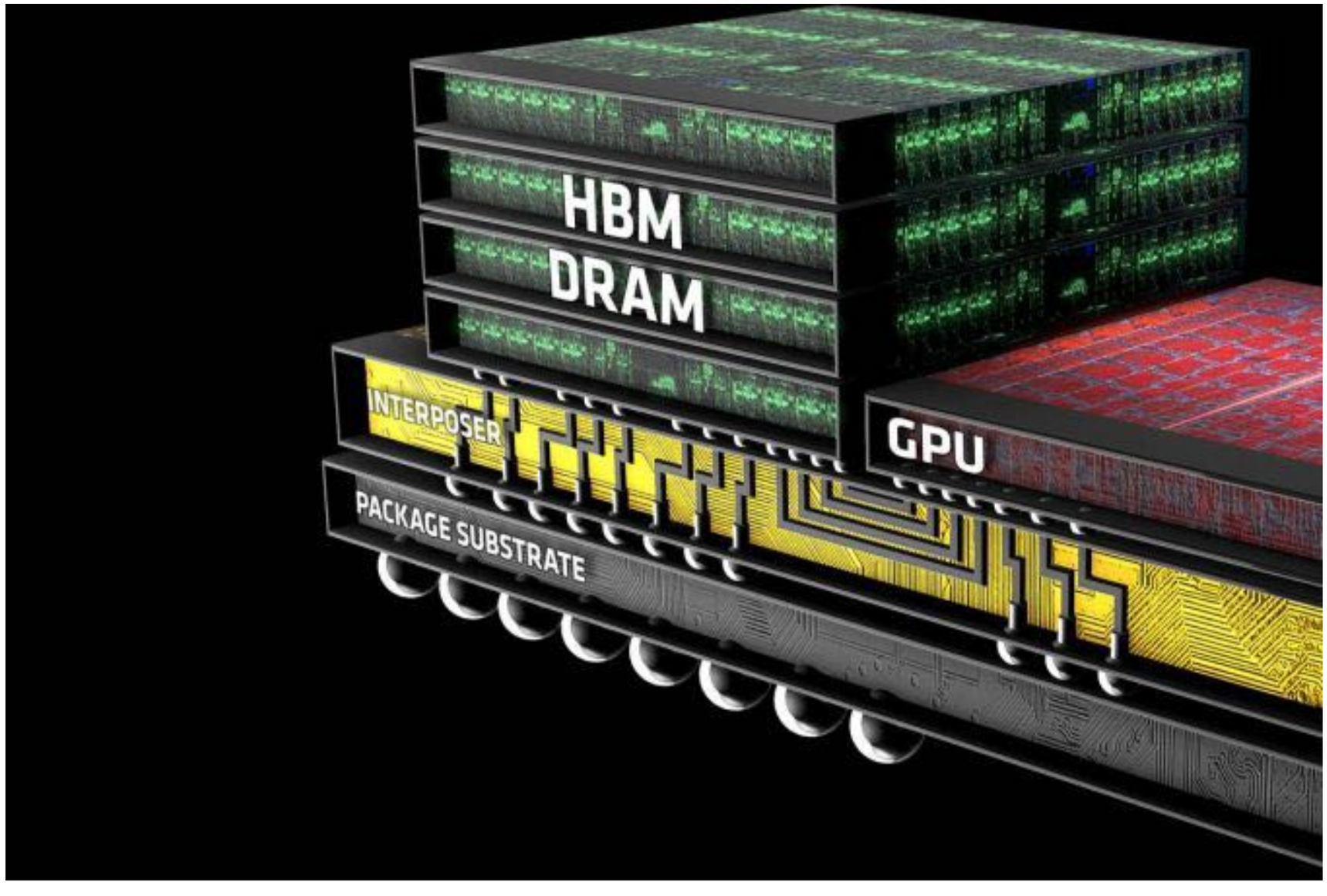
Solution: Multi-Core MCM Processors

- AMD Zeppelin SoC targeting server market
- FinFET 14 nm
- 4x die multi-chip module (MCM)
- 8x Zen cores per each die
- L3 cache 16MB
- 32x high speed serdes lanes
- Similar monolithic chip (32x cores) would cost 70% more than 4x smaller chips
- Yield of making MCM much better than yield of large size chips (expected size 777 mm^2)



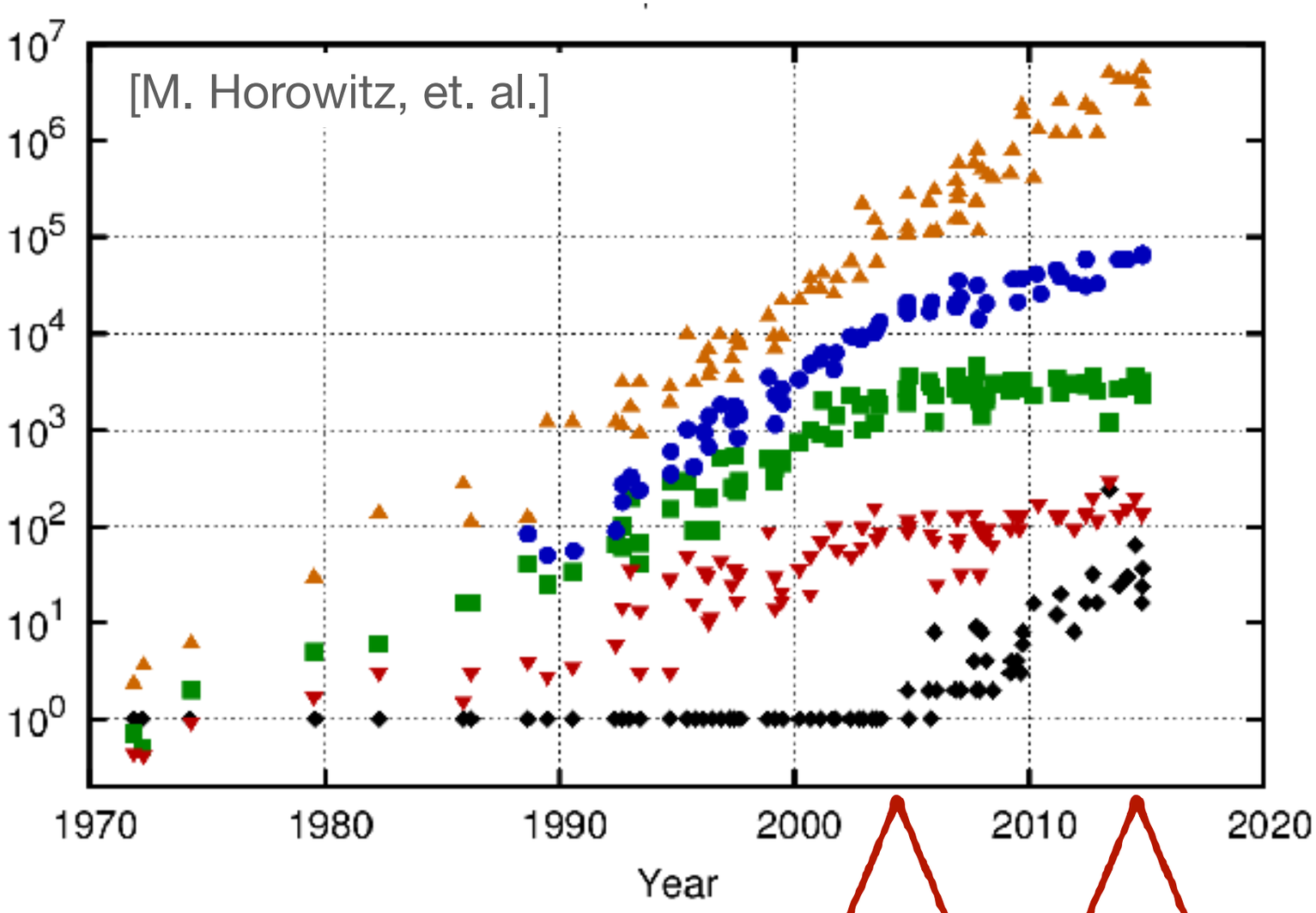
[AMD, ISSCC'2018]

Processing Power: Yield and Cost

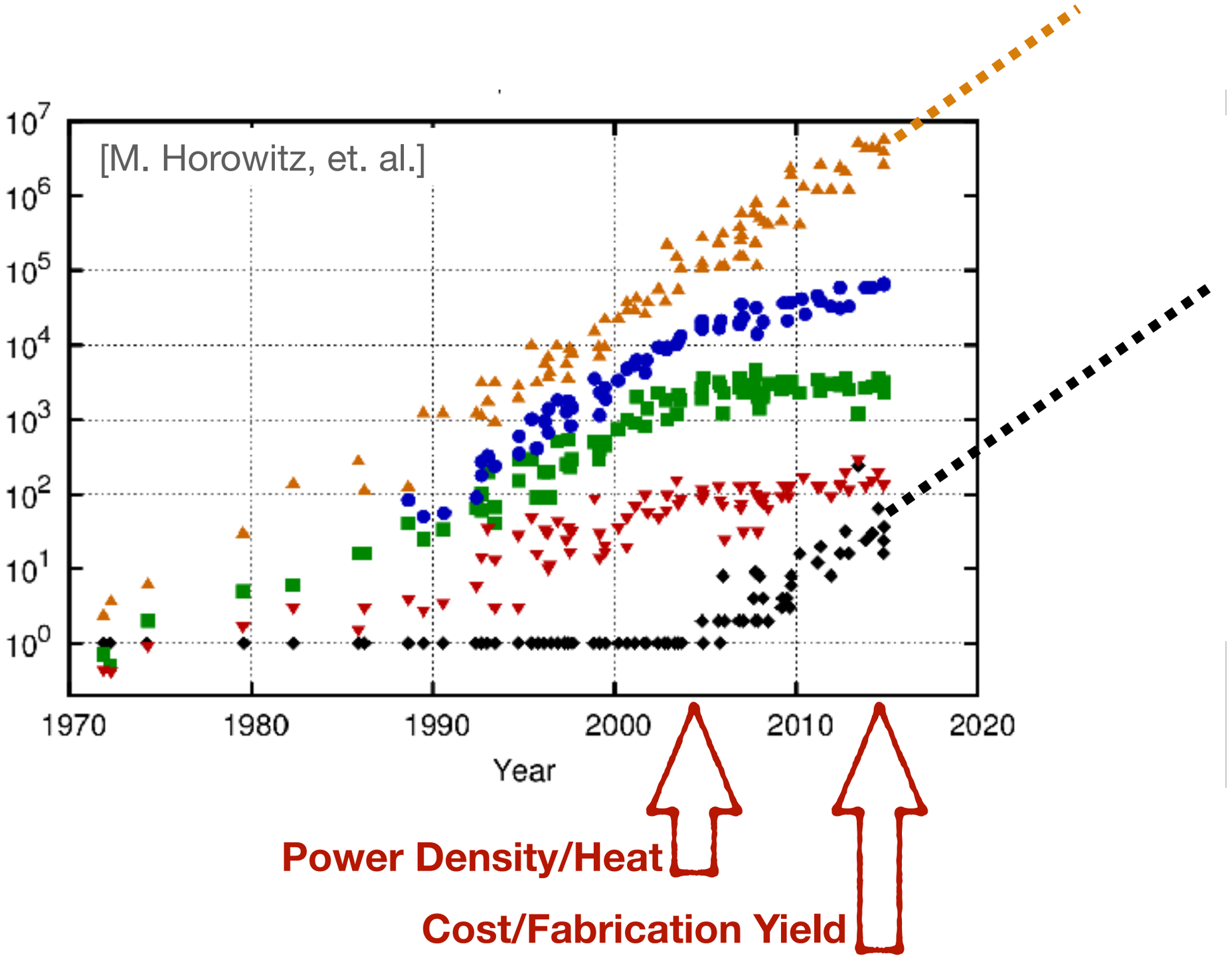


[intel.Com]

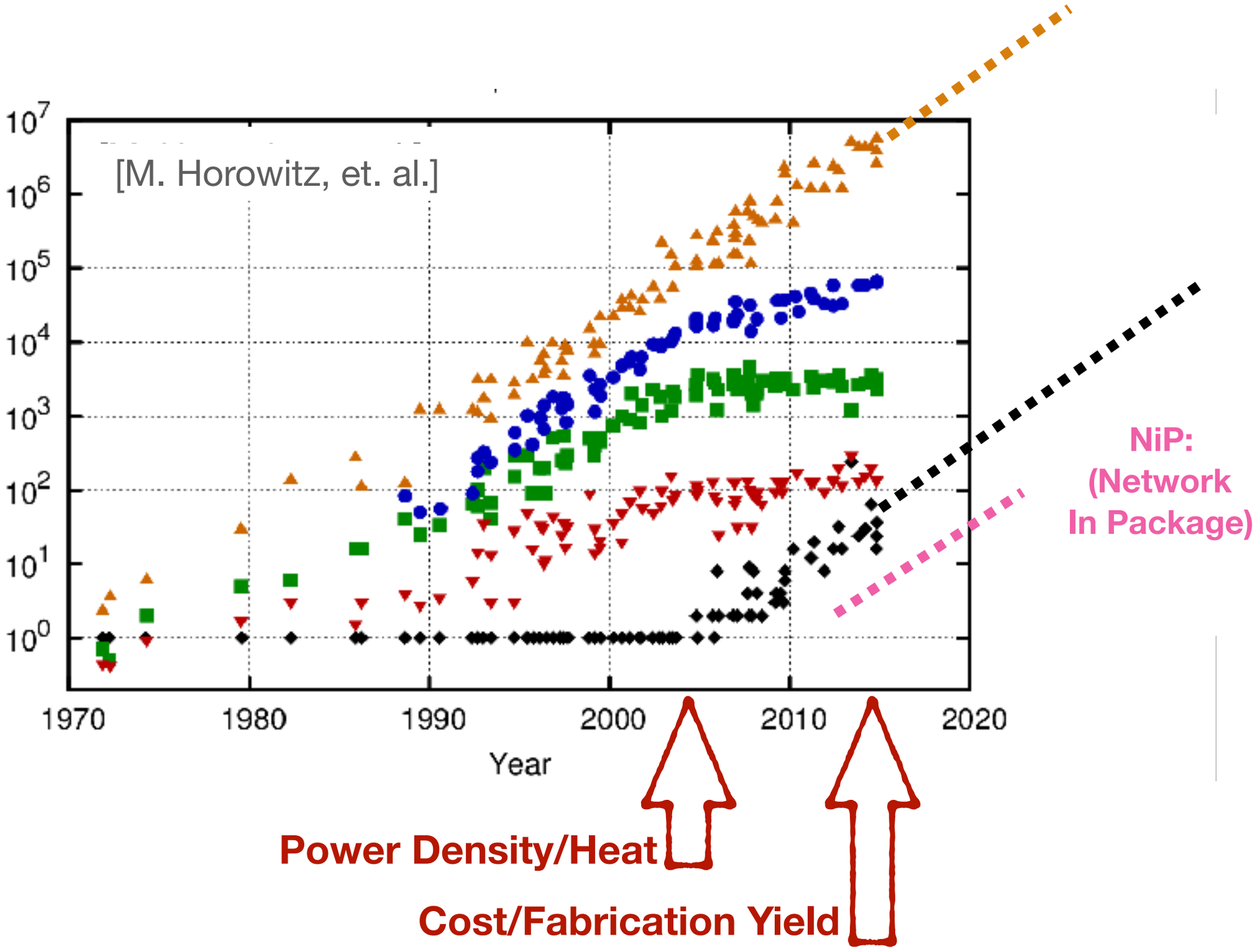
Processing Power: Observations



Processing Power: Observations

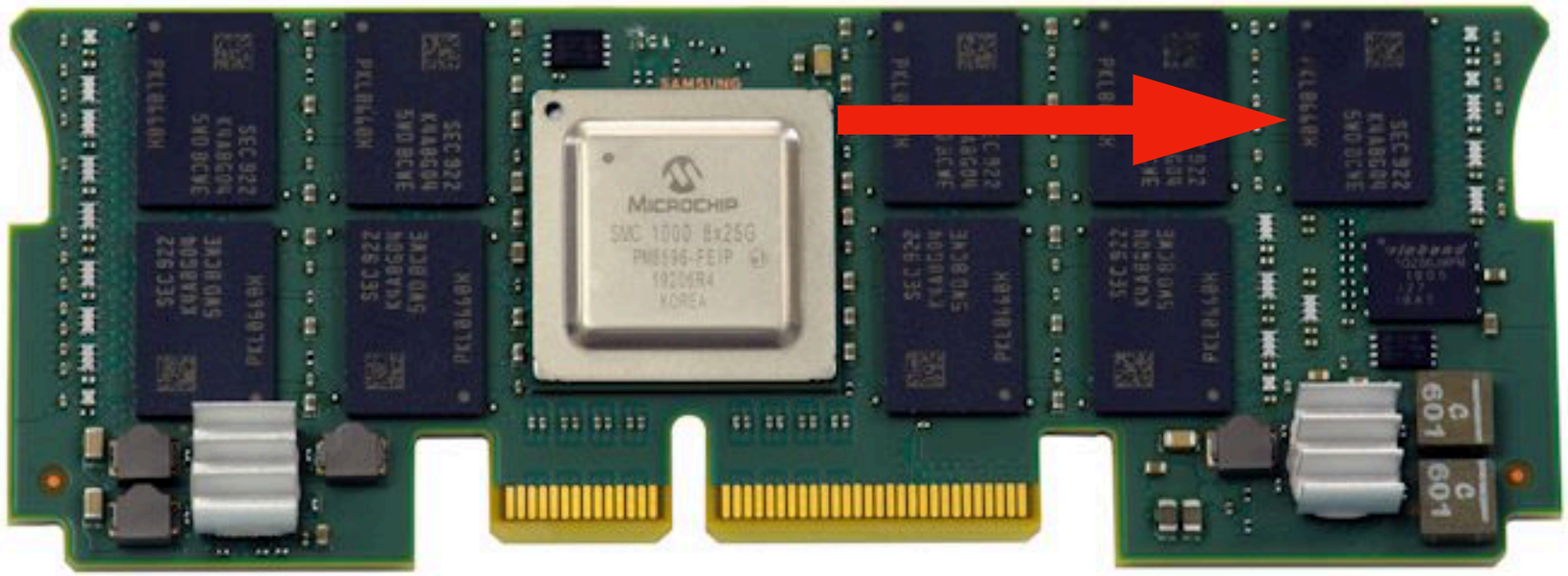


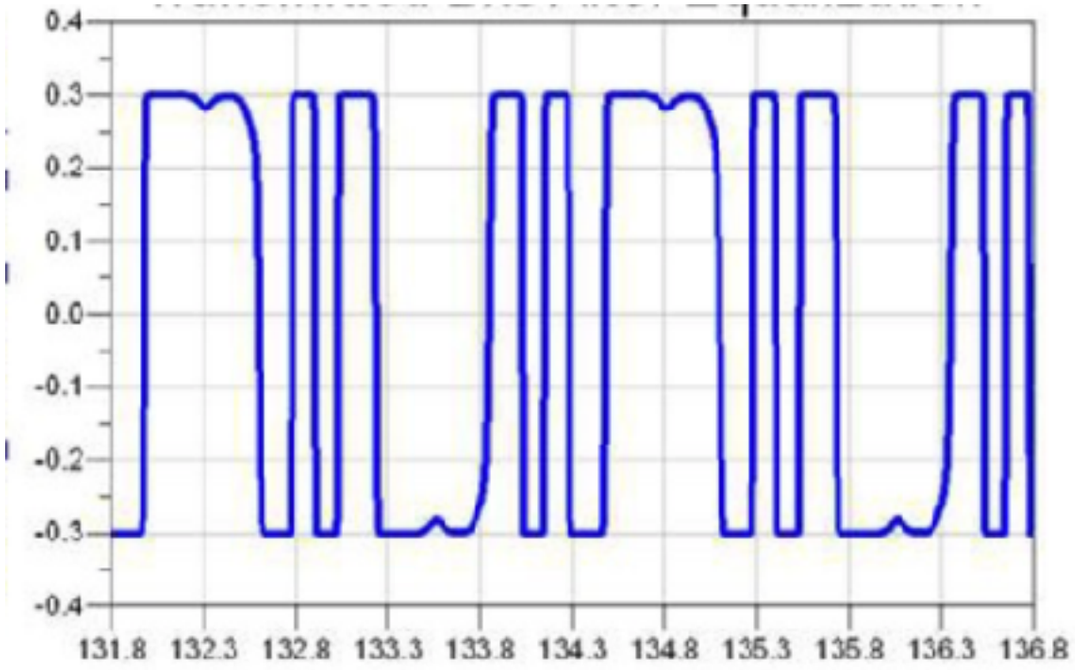
Processing Power: Observations

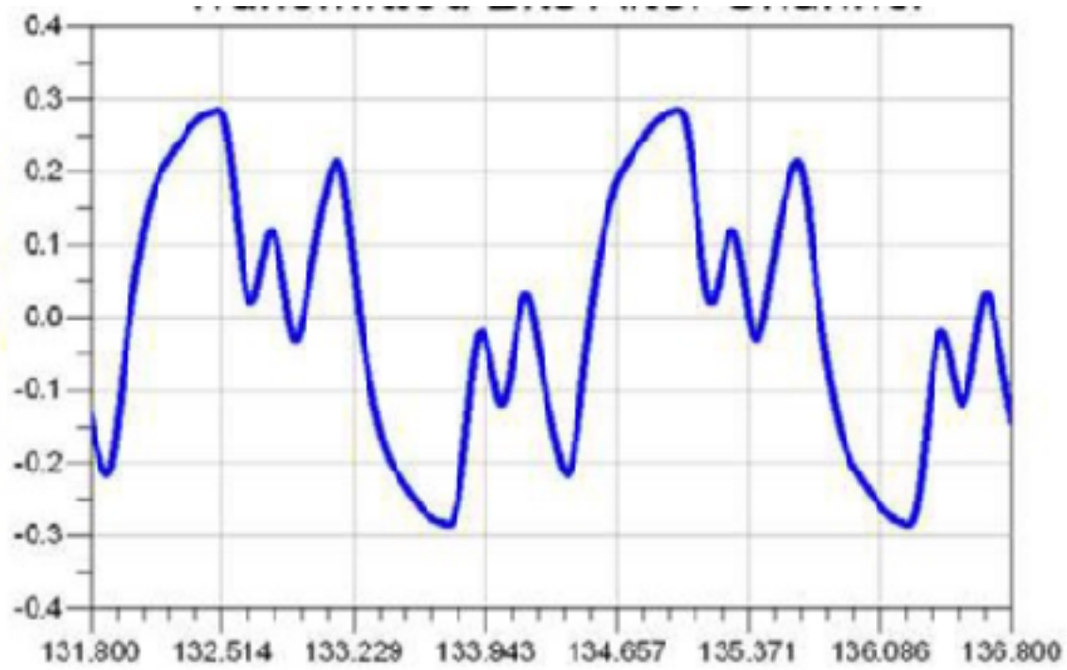


[A. Tajalli, IEEE SSCM 2019]

Copper Channel to Carry Data

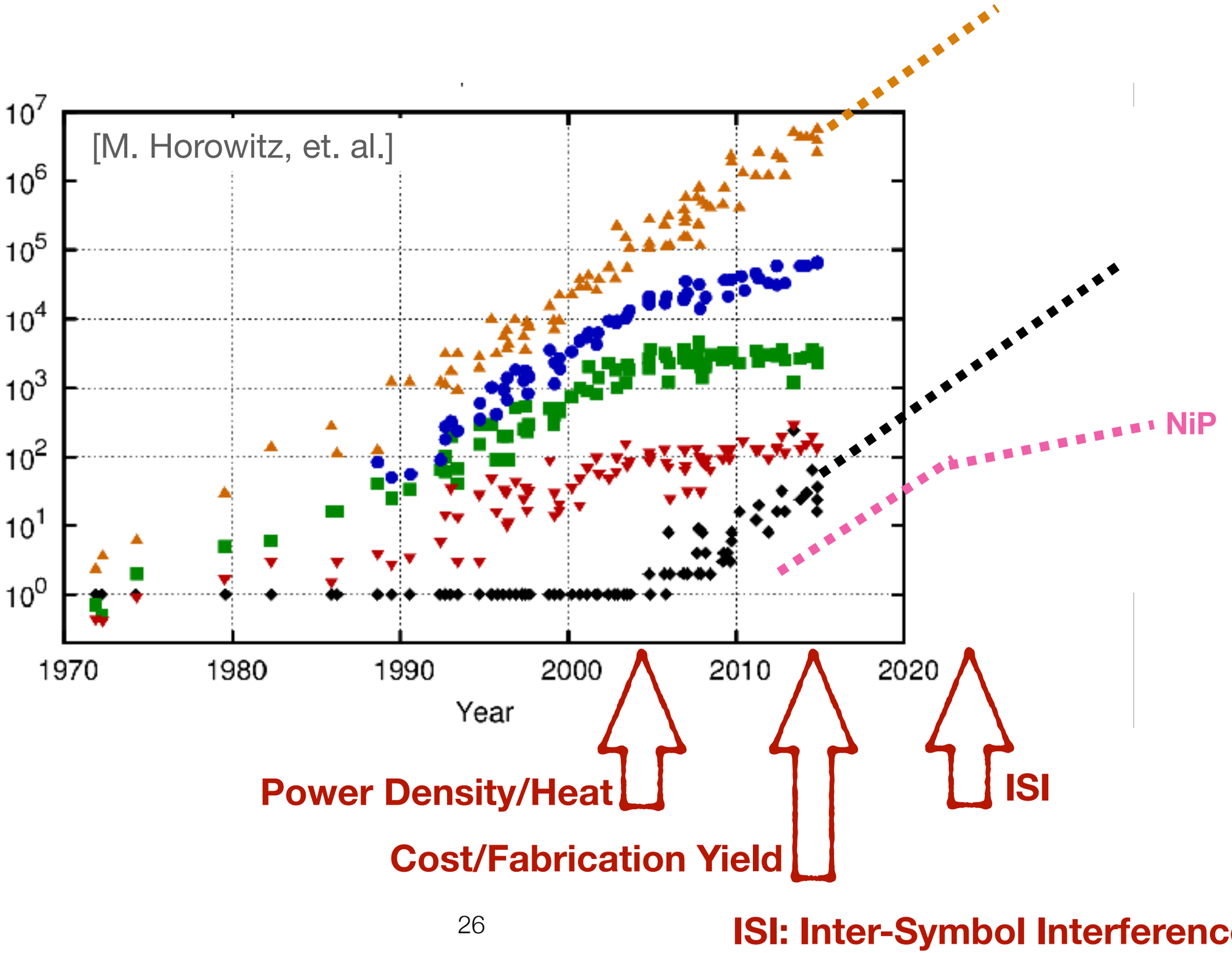




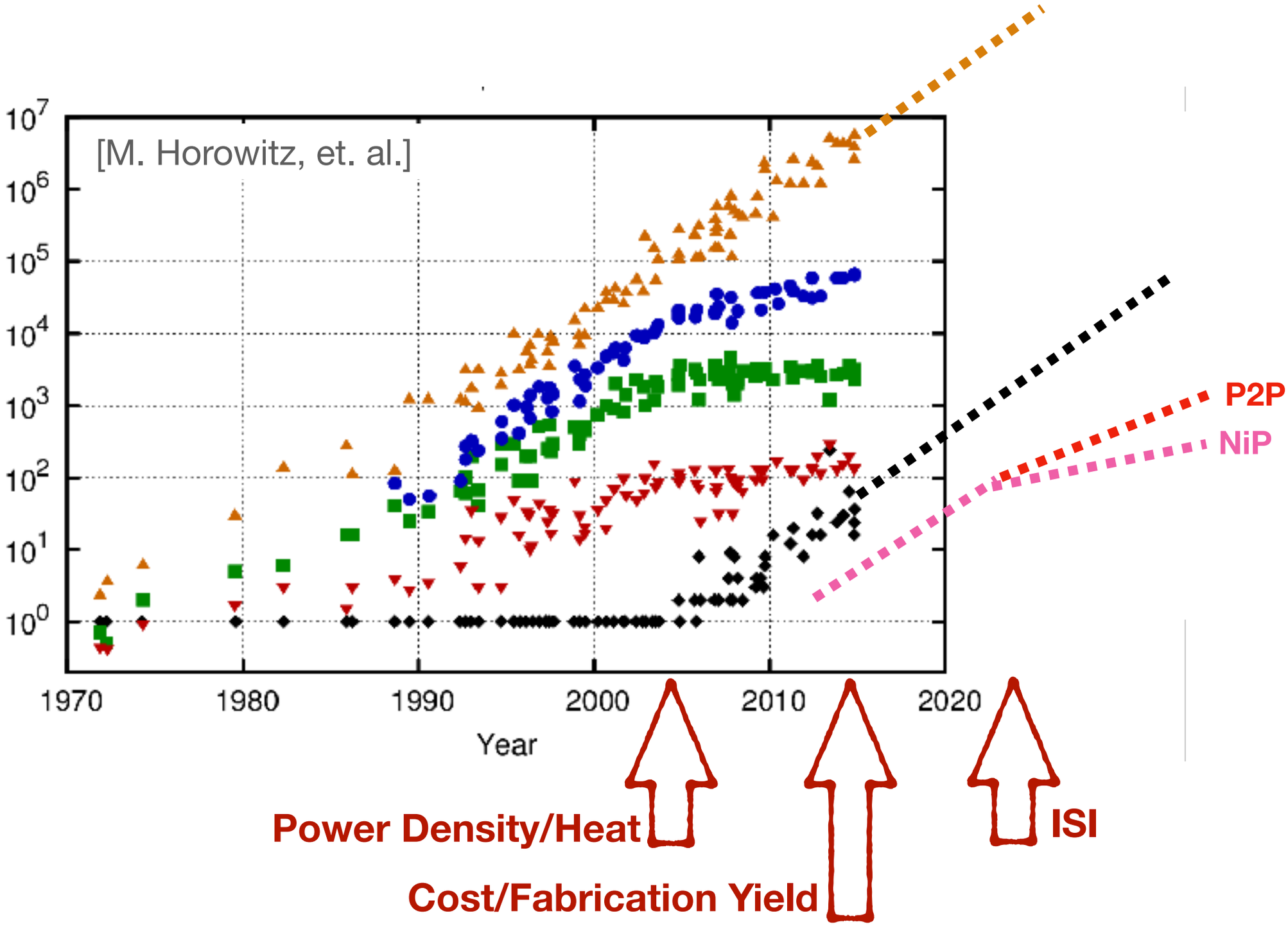


Needs pattern recognition !

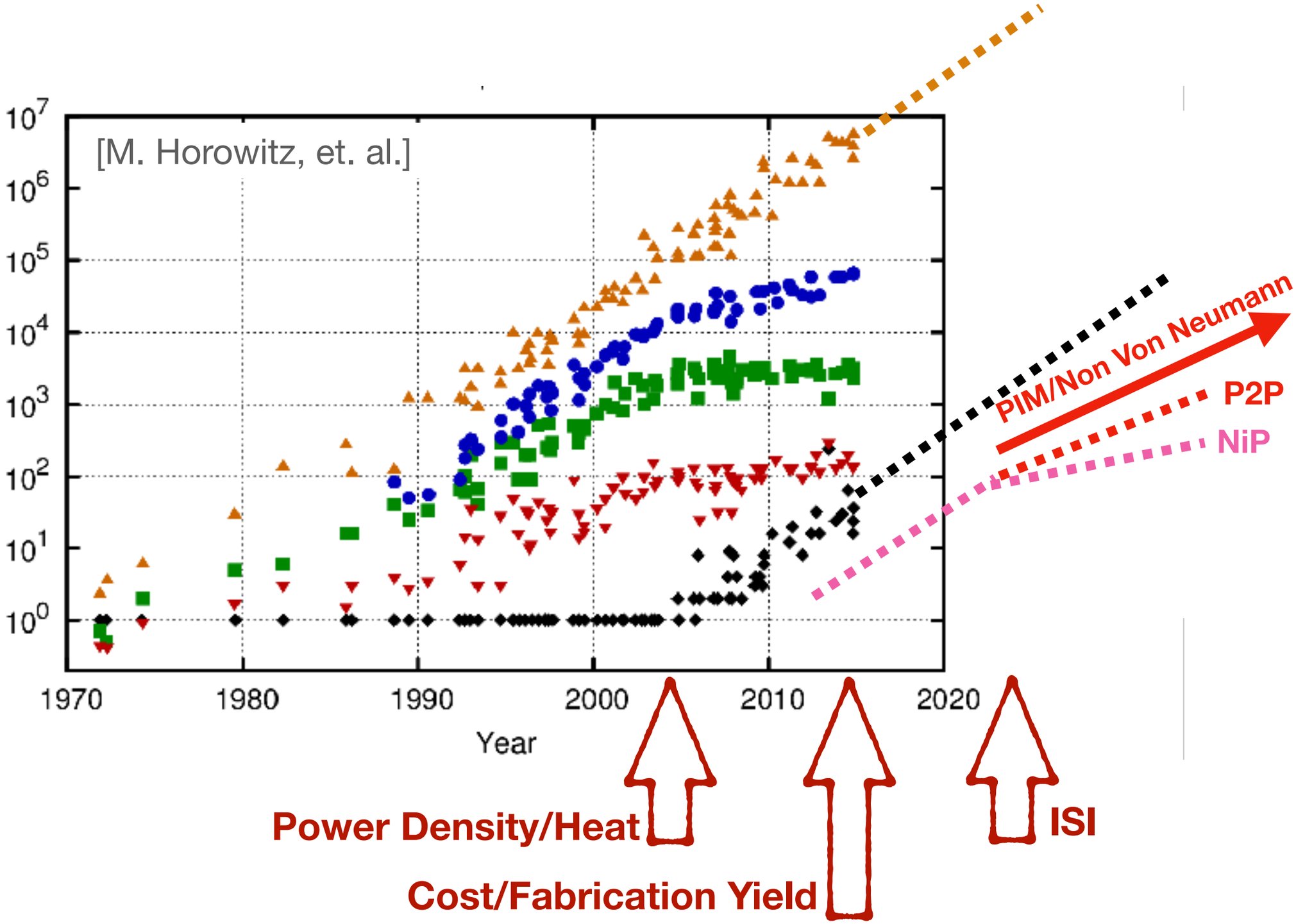
Processing Power: Observations



Processing Power: Observations



Processing Power: Observations

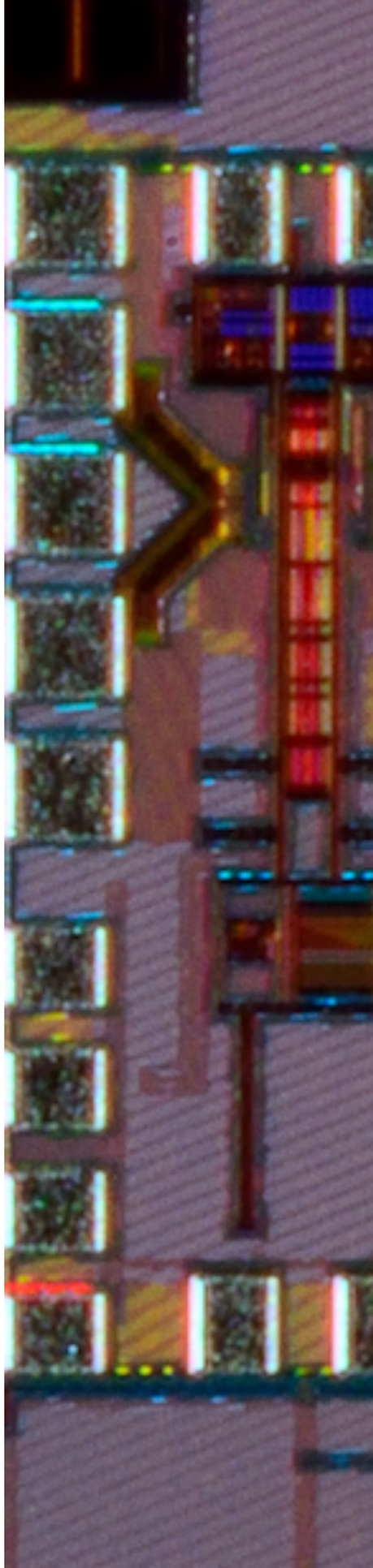


Processing Power: Key Observations

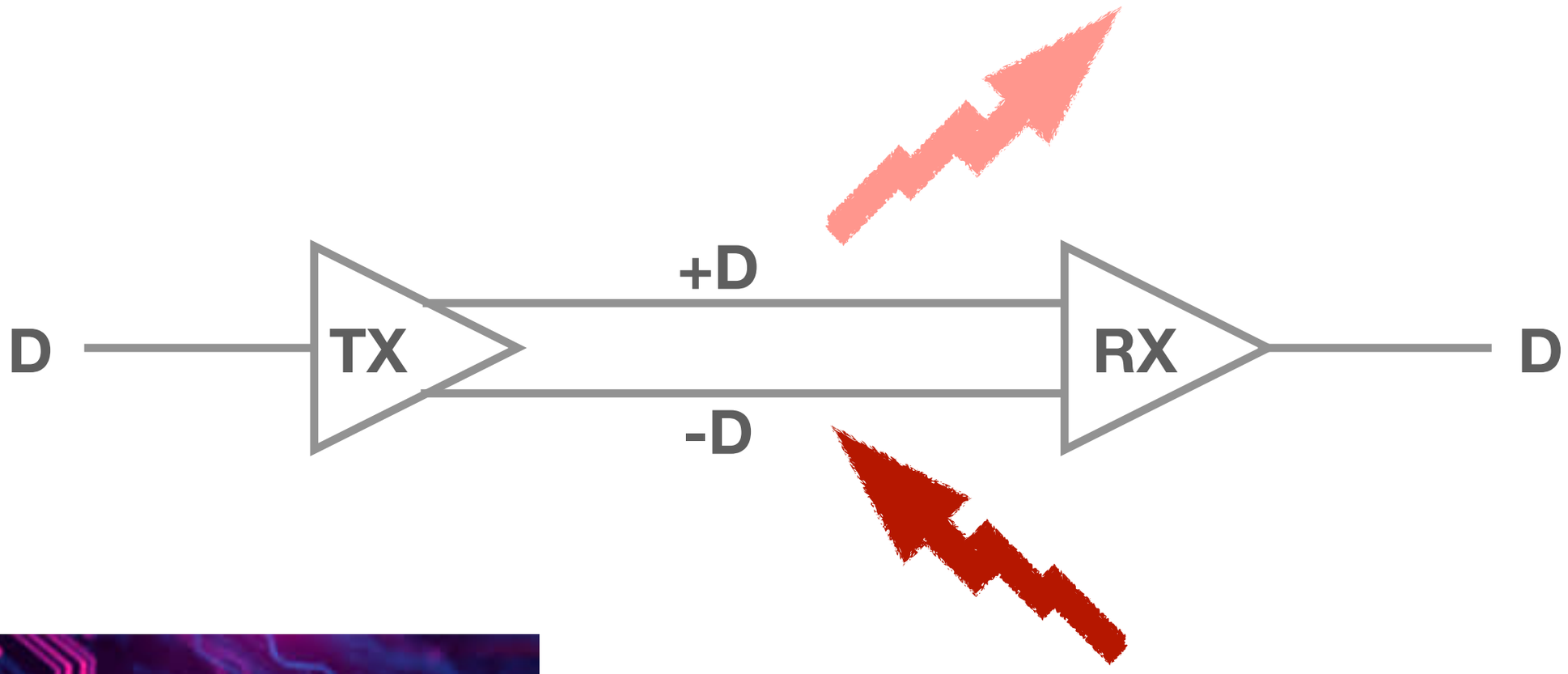
- Advanced **Coding** and **Communications** schemes have been employed in the past two decades in order to improve **Computing Power** against physical barriers such as:
    - Heat and power density
    - Yield and cost

- Advanced Coding and Communications rely on:
    - High-performance signal processing techniques
    - **Circuit/Coding theory** provides the right algorithms to implement advanced signal processing techniques.

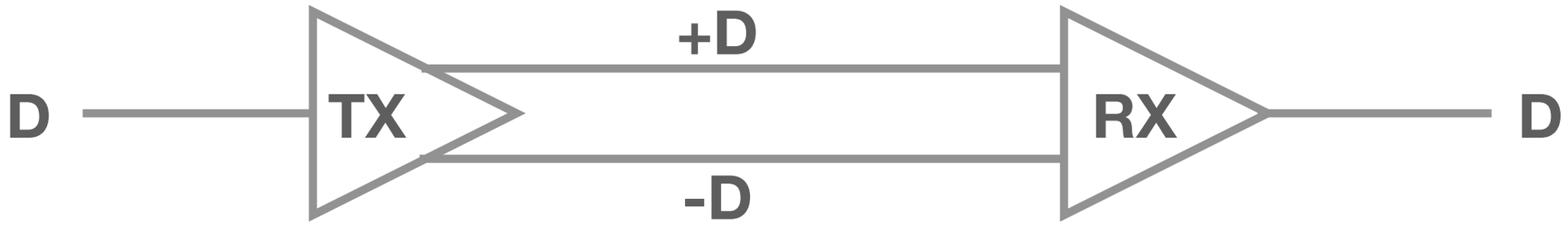
Communication for Computation
Hadamard over Wire



Differential Data Transmission



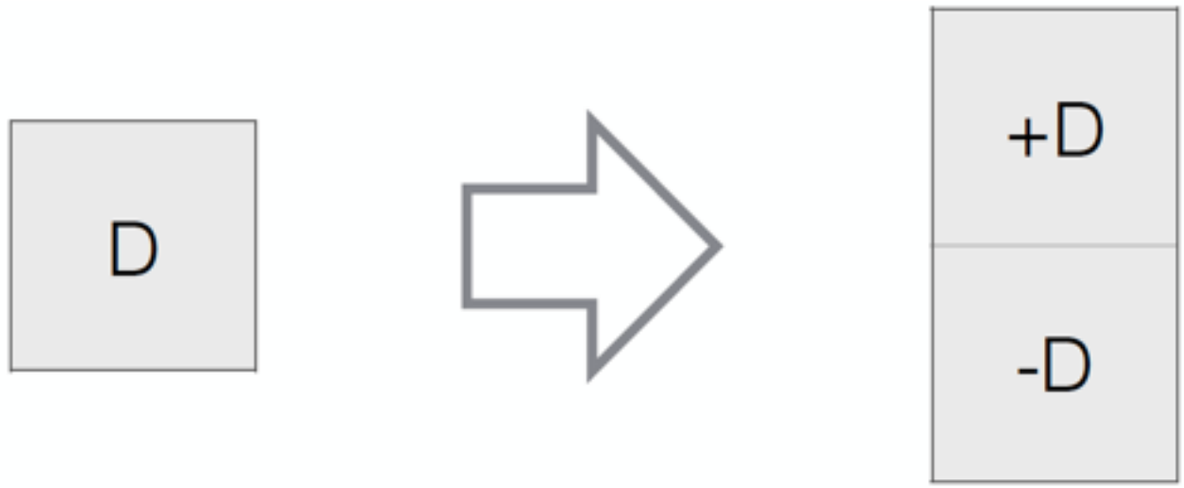
Differential Data Transmission



Differential signaling

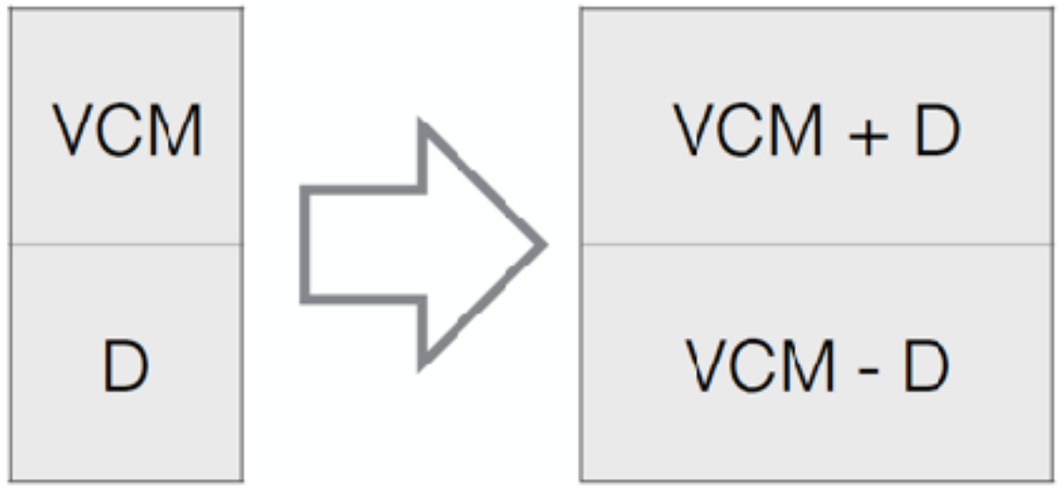
- Produces very little data dependent noise
- Low sensitivity to cross-talk
- Robust, however requires two wires to carry one bit

Differential Data Transmission



Single ended to differential conversion

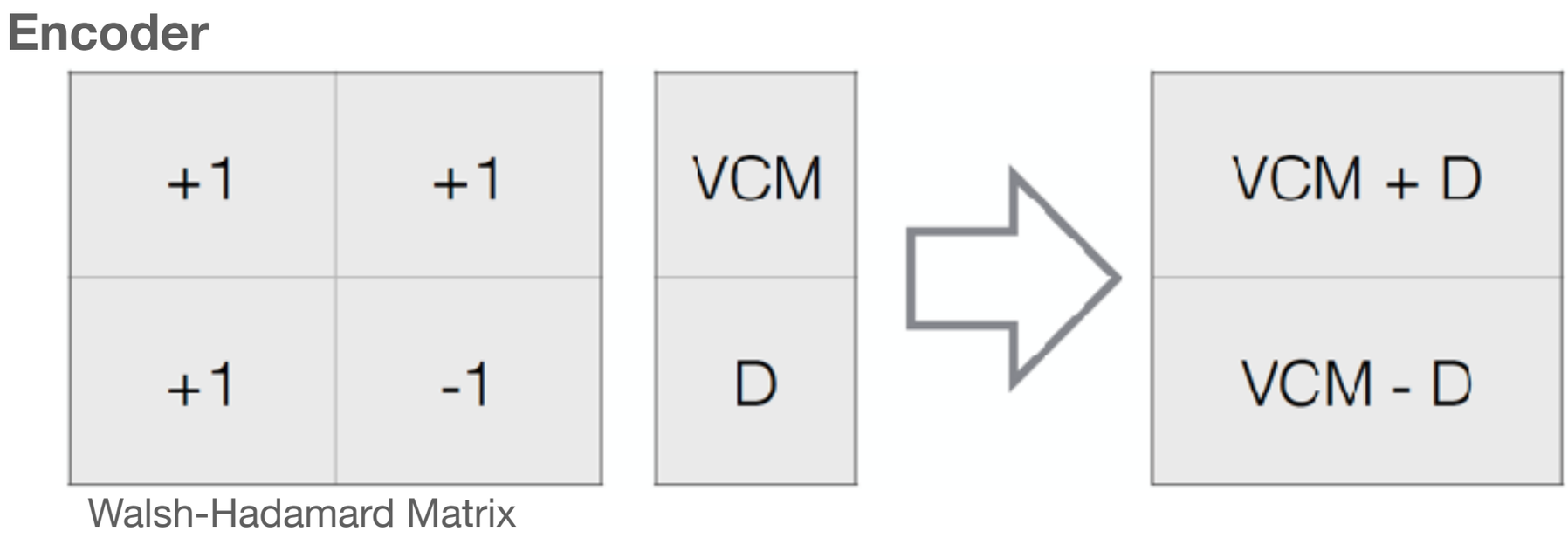
Differential Data Transmission



Properties of differential signaling:

- Robust against crosstalk, supply noise, and common mode noise
- Produces no supply noise SSO
- ISI ratio is ONE

Differential Data Transmission: Encoder



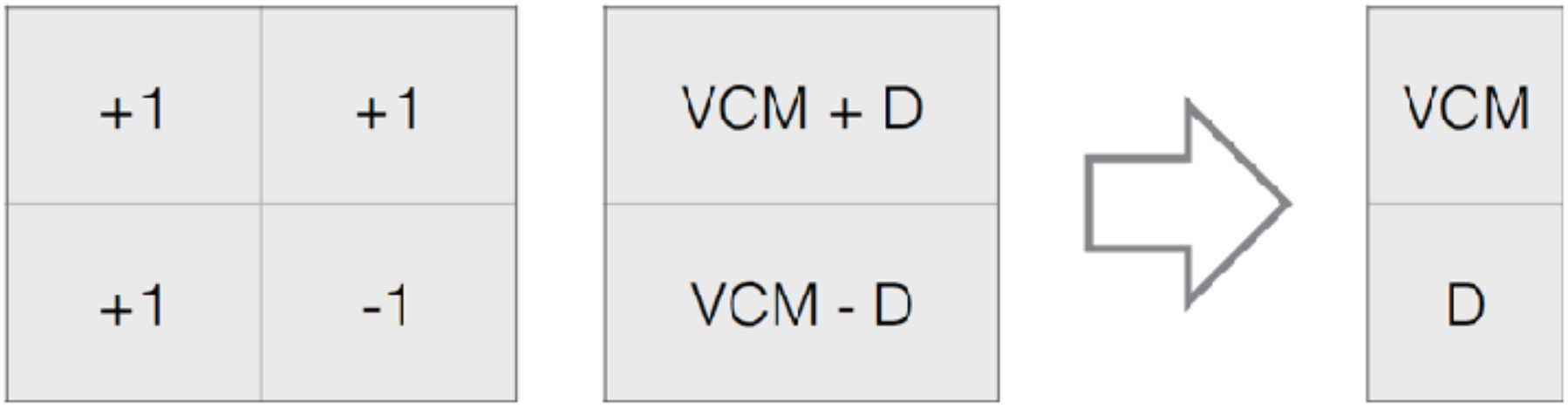
Properties of differential signaling:

- Robust against crosstalk, supply noise, and common mode noise
- Produces no supply noise SSO
- ISI ratio is ONE
- Puts 1b over 2 wires

[A. Shokrollahi and A. Tajalli, 2011]

Differential Data Transmission: Decoder

Decoder



Walsh-Hadamard Matrix

Generalized Form

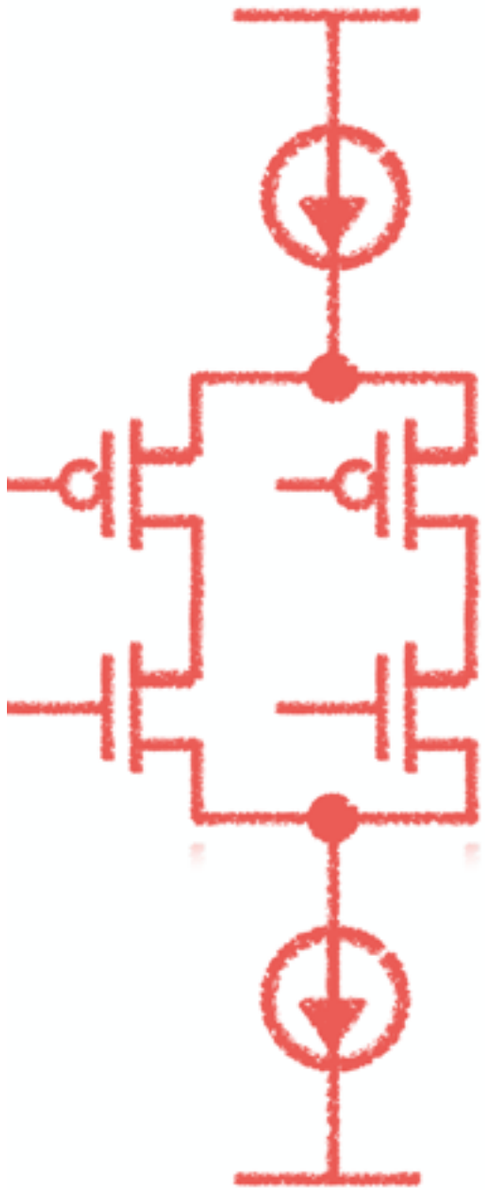
H	H
H	-H

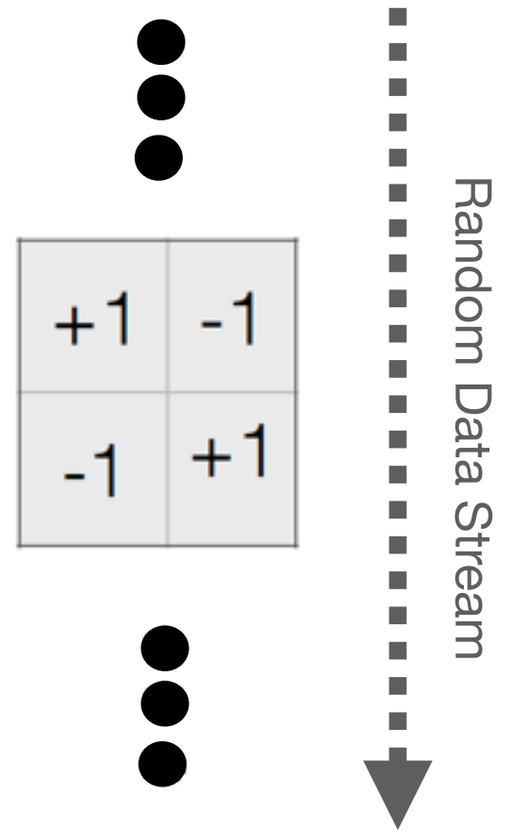
H: Walsh-Hadamard Matrix

Properties of differential signaling:

- Robust against crosstalk, supply noise, and common mode noise
- Produces no supply noise SSO
- ISI ratio is ONE
- Puts N bits over N+1 wires

MIMO Over Wire: Circuit Topology

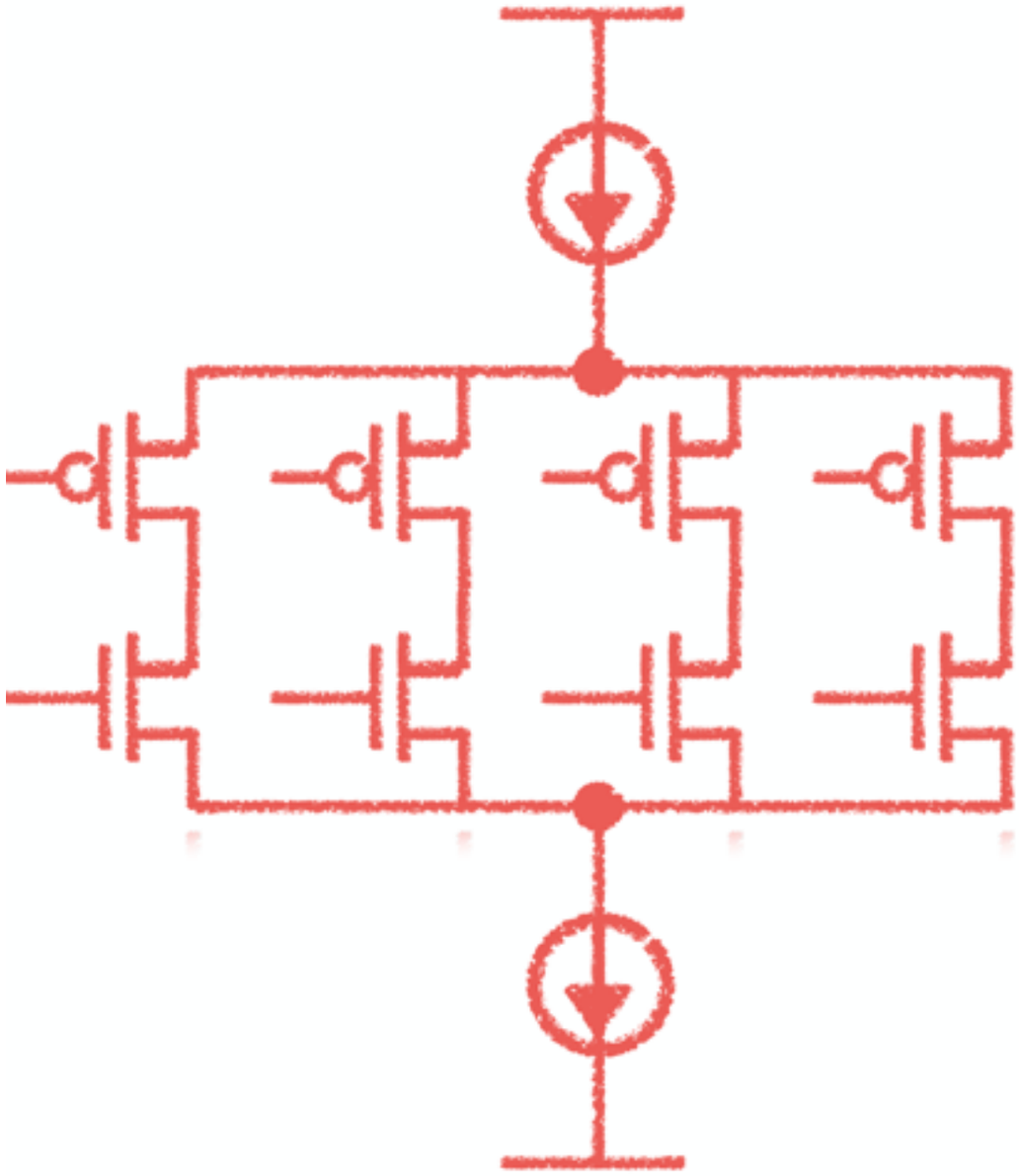




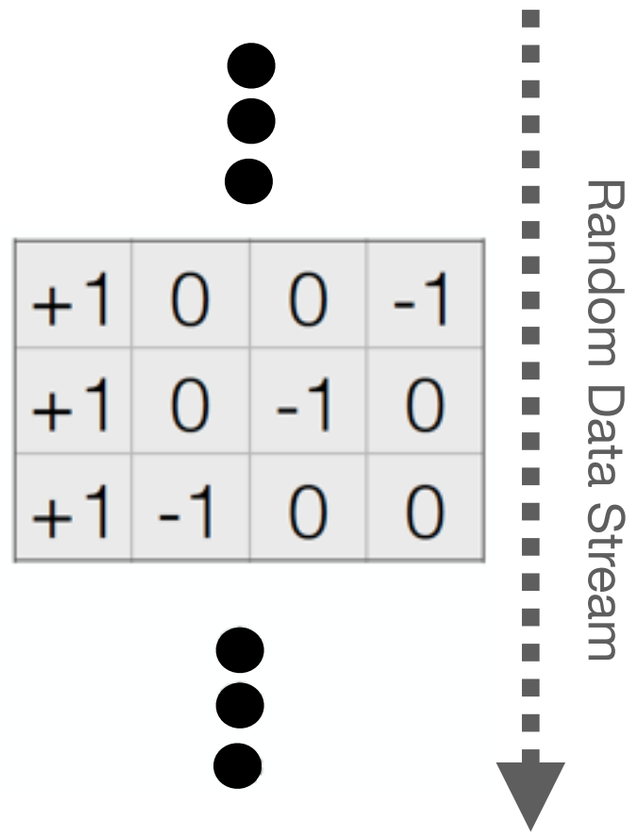
Example of a conventional differential driver/receiver

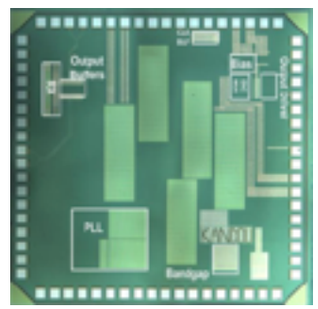
[Tajalli et al, JSSC, 2008]

MIMO Over Wire: Circuit Topology



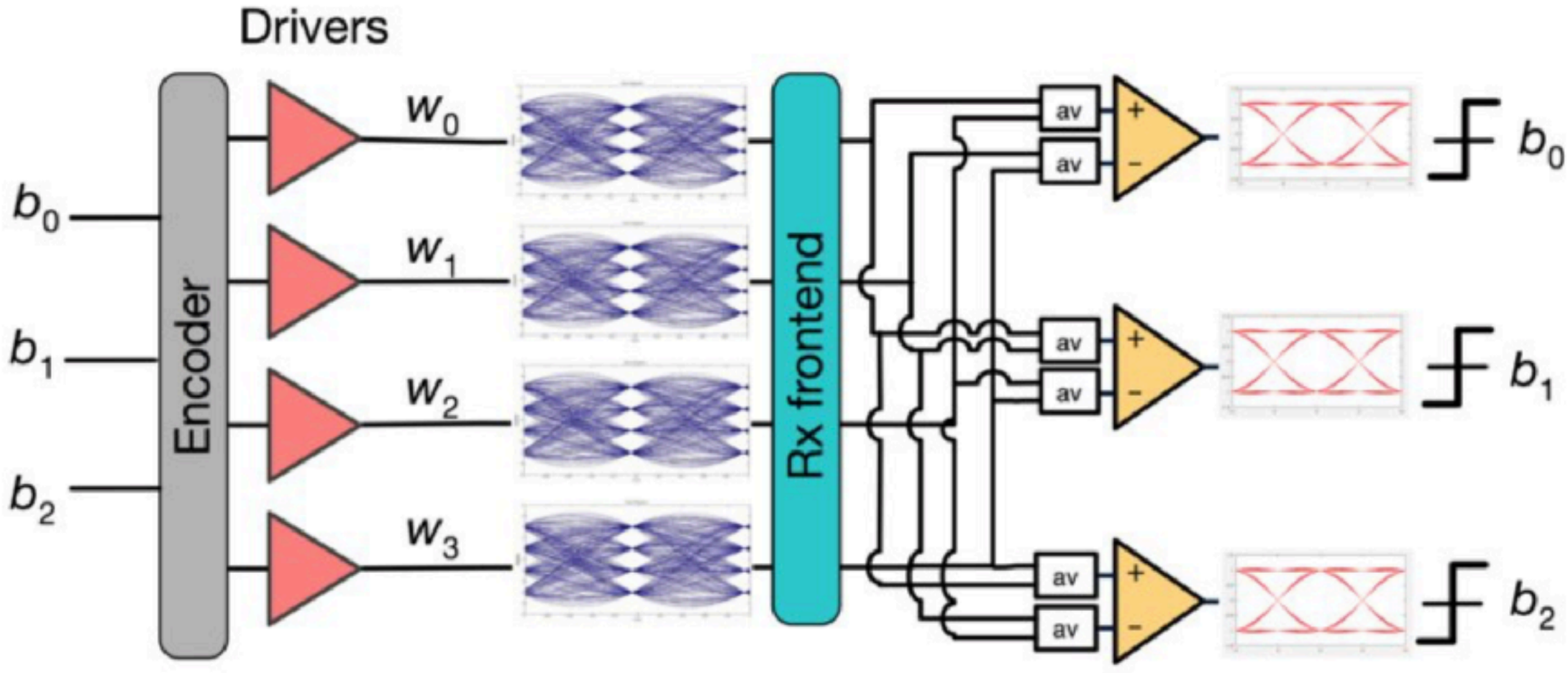
Example of a multi-wire balanced driver/receiver





[Tajalli et al, US Patent, 2011]

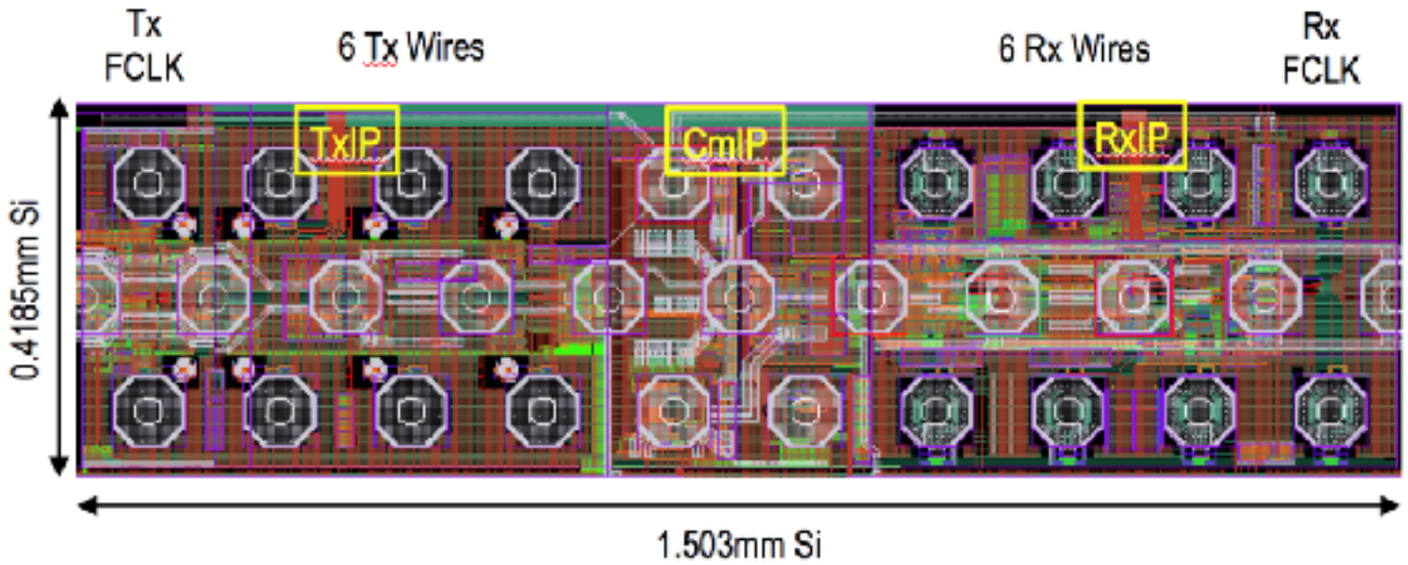
MIMO Over Wire: Analog Matrix Transformation

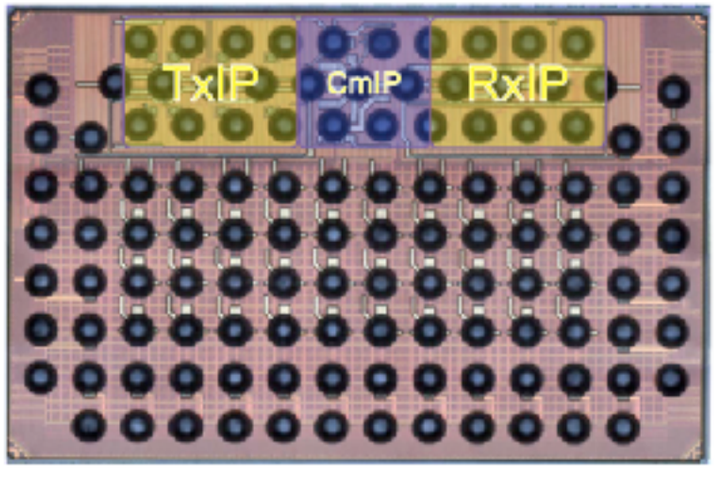


[Tajalli et al, US Patent, 2011]

MIMO: Generalized Differential Signaling

- CMOS 28 nm
- 5b/6w
- 125 Gb/s over 6 wires
- 25 Gb/s over each wire
- Forwarded clock line
- PLL BW: 600 MHz
- Energy consumption of TRX: 0.96 pJ/b
- Comparison:
  - Nvidia, 1.17 pJ/b 16 nm, ISSCC'2018
  - AMD, 2 pJ/b 16 nm, ISSCC'2018

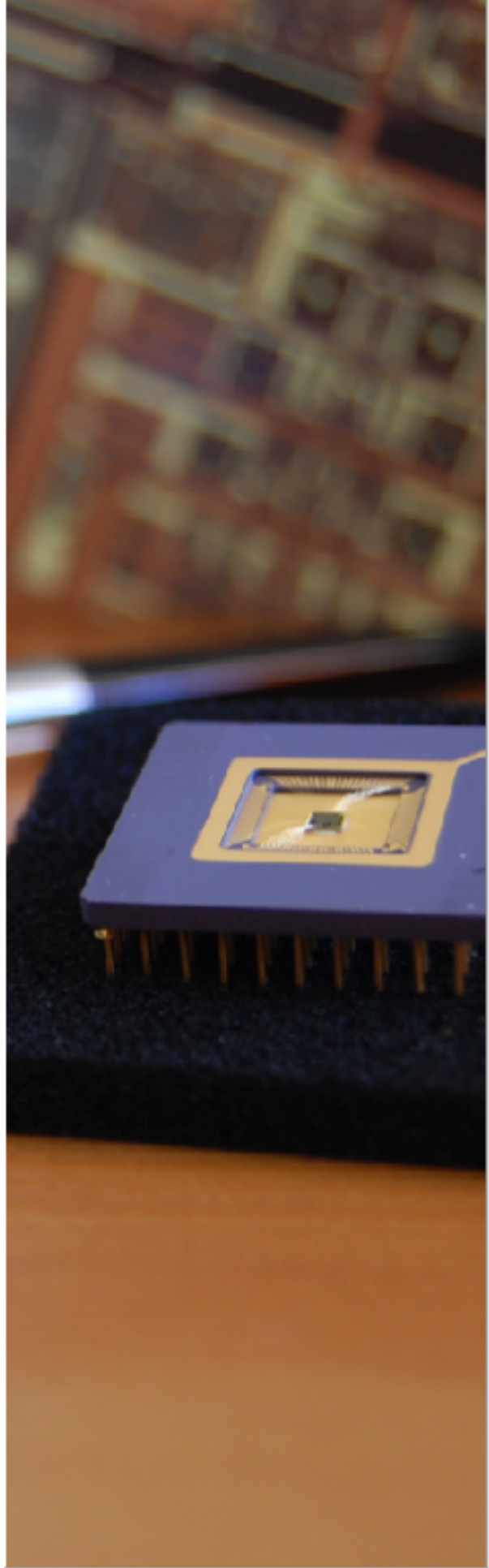




[ISSCC, 2016]

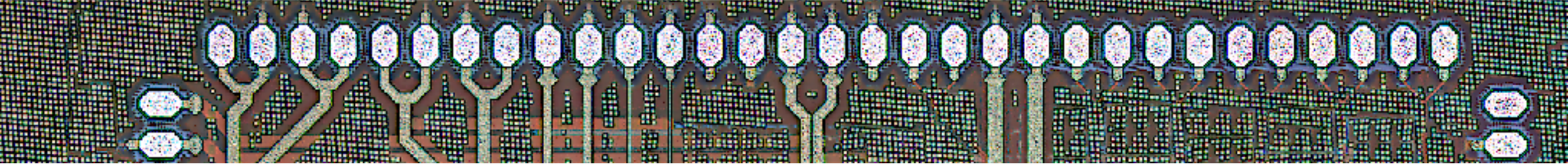
Communications, Computation, and Circuits

Conclusion



Summary

- High performance computing needs innovation; especially in hardware.
- Applications such as Machine Learning do need different computer architectures; in which extremely high throughput communication is a key enabling technology.
- Future processors seek for faster physical devices, and will be equipped to high-speed communication links.
- Circuit designers map complex communication and signal processing schemes into geometrical topologies to implement such processors.
- Faster communication needs solid understanding on Coding and Computing.
- Future circuit designers should have a very deep knowledge and understanding on information technology (coding, communications, signal processing, etc).



LCAS Employs Advance Signal Processing, Communications, and Coding For Extreme High Performance & Energy Efficient Circuit Design

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