DESIGN AUTOMATION FOR SILICON NANOPHOTONIC INTEGRATION

D2T SYMPOSIUM SEMINAR
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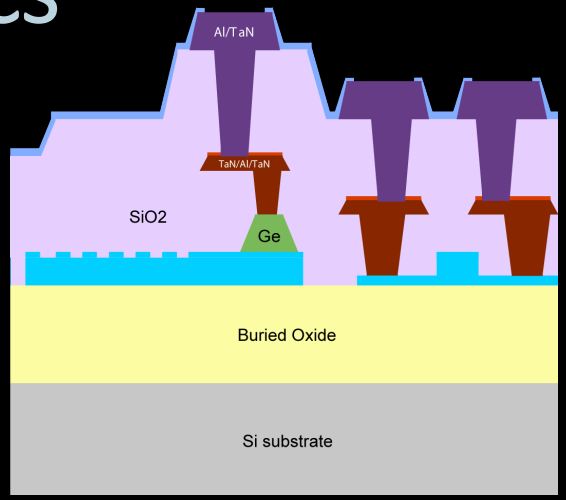
Priyank Kalla
Collaborators: Chris Condrat, Lawrence Schlitt & Steve Blair

THE UNIVERSITY OF UTAH

Agenda

- In Context: Integrated Optics
  - Silicon Photonics Devices and Application
  - Motivation for Design Automation
- Background
  - Integrated Optics and Waveguide Devices
  - Signal Losses in Integrated Optics
- Design Automation for Integrated Optics
  - Logic Synthesis
  - Physical Design Automation
  - Thermal-aware Synthesis and Integration
- Conclusions, Future Work

In Context: Integrated Optics



Silicon Photonics
- Optical integration into semiconductor processes
- High-speed optical communications in silicon

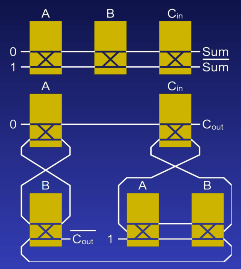
Architectures
- Photonic networks on chip
- 3D ICs; Communication layers
- Photonic Interconnects, WDM

Applications Beyond Telecom
- Switching, sensing, filtering, quantum

Convergence of Communications and Computation
- Signal processing, optical synthesis, optical computing

Necessity of Design Automation
- Logic Synthesis & Physical Design
- Thermal-aware design automation

OpSIS Initiative – Univ. of Delaware, AFOSR
- MOSIS for optics
- Integrated optics practical for experimentation
- Library elements as building blocks; PDK available



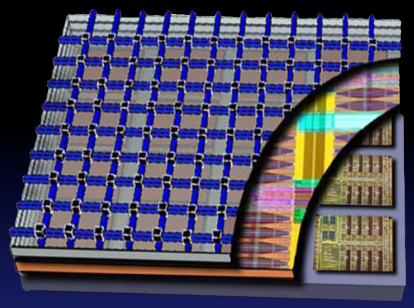
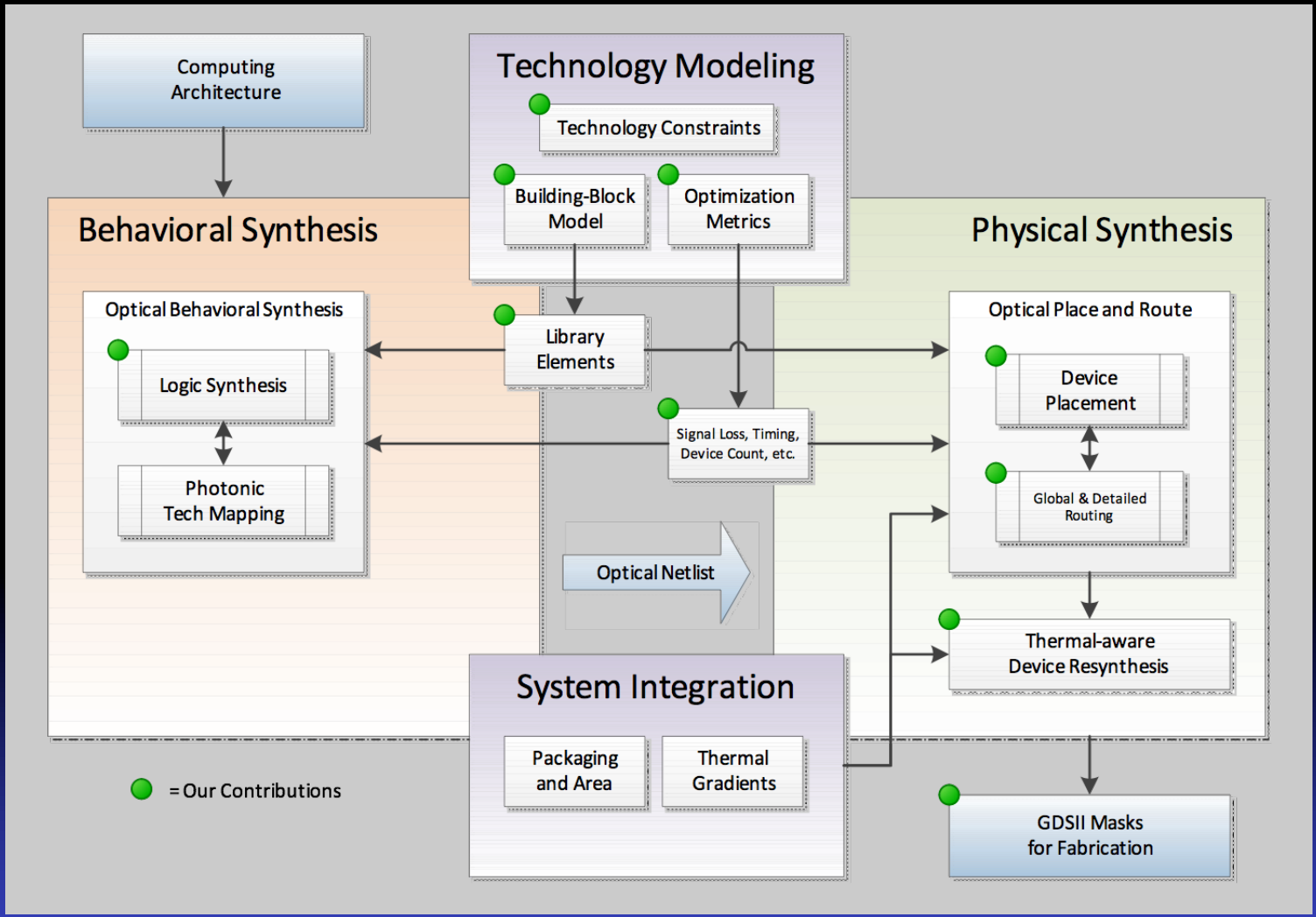


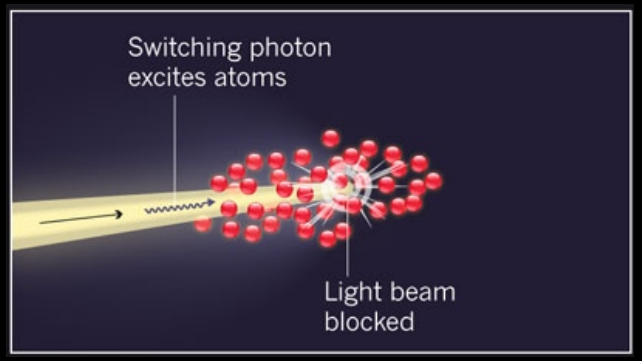
Image credit: IBM

Our Design Flow

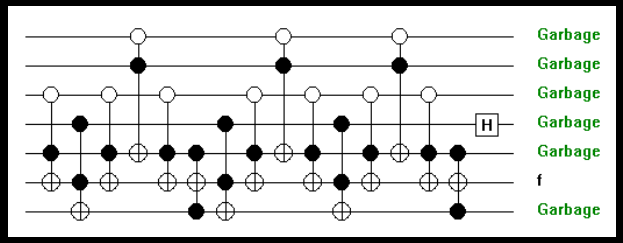


Logic Devices and Behavioral Synthesis

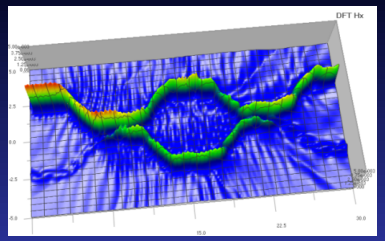
- Optical Computing
  - AFOSR, MURI, OpSIS
- Current Art and Challenges
  - Optical "transistors"
  - Optical gate research
  - Reversible logic, quantum
  - Challenge: Nonlinearity + amplification
- Conventional Switching Devices
  - Switching logic elements
    - Electrically controlled optical switches
    - MZIs, ring-resonators, etc.
    - "Directed Logic" (Hardy, Shamir, Caulfield, et al)
- Switching as logic *abstraction*
  - Logic synthesis, scalability, composability

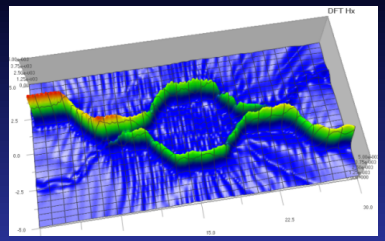


"All-Optical Switch and Transistor Gated by One Stored Photon", W. Chen, et al, Science Magazine, 2013

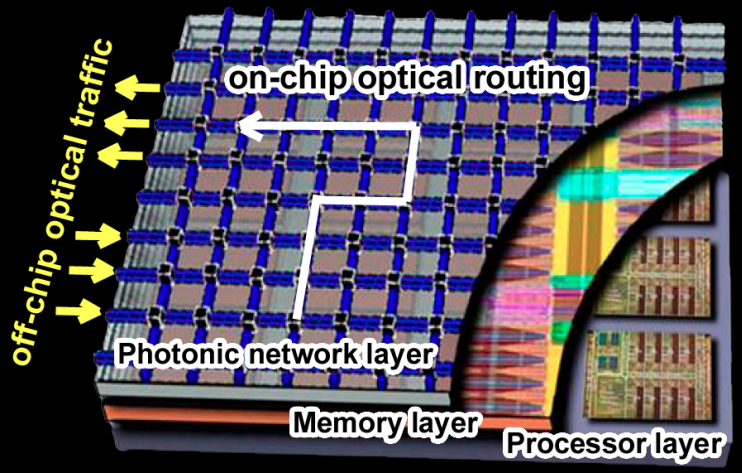


- Our Contributions:
  - Optical switching logic composition methodologies
  - Multi-level logic synthesis
  - Physical design methodology + Detailed routing

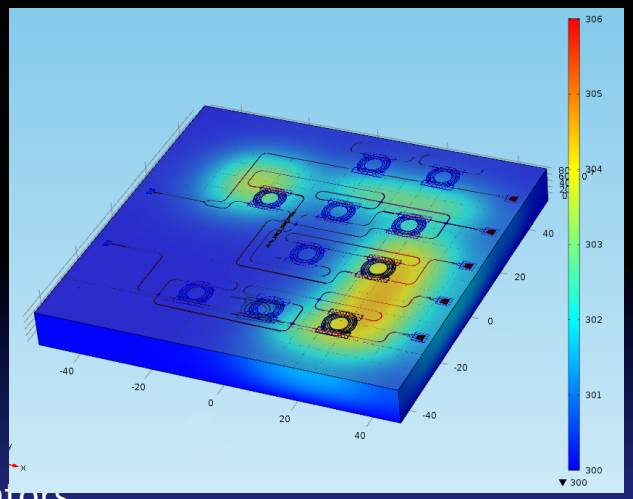




Thermal-aware System Integration

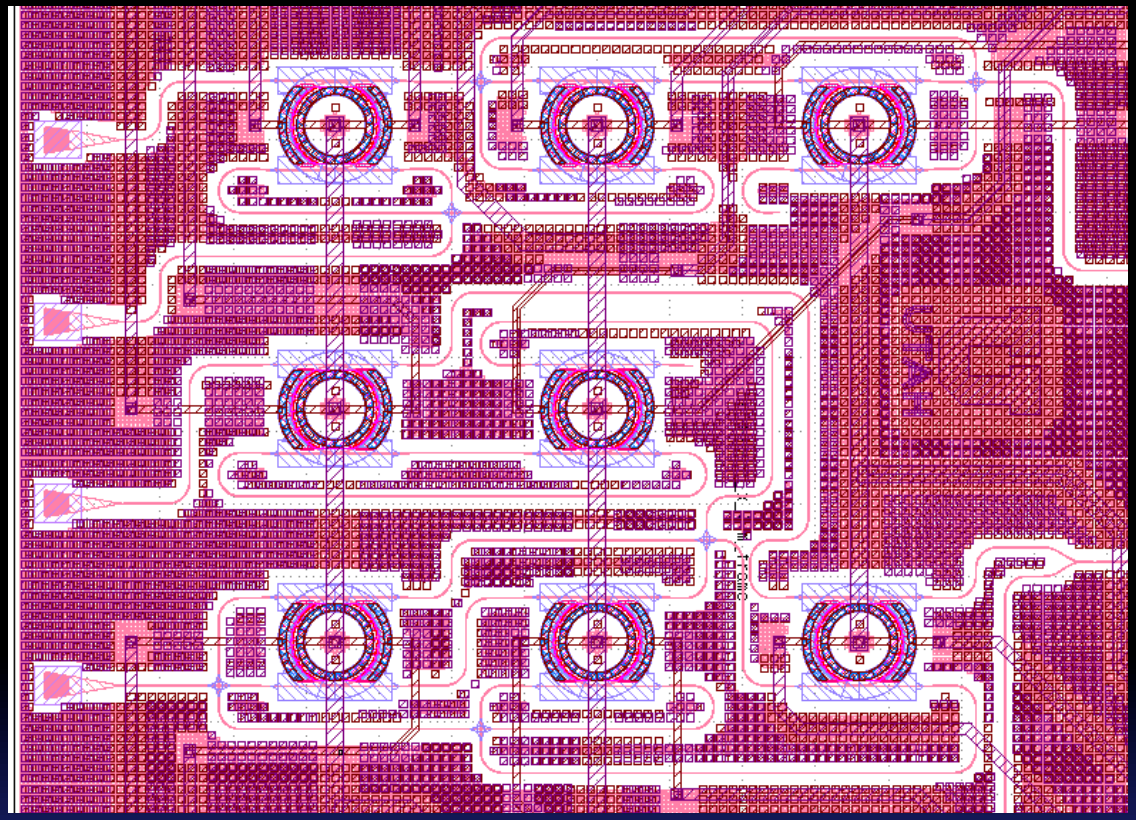


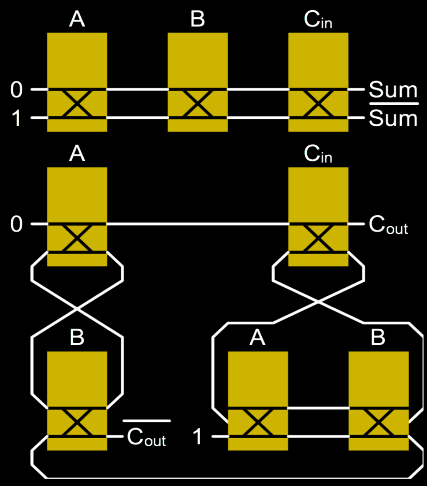
- Optical Networks-on-Chip
  - Ring Resonators = Device of choice
    - Small, sensitive, fast, high-Q
  - But….
- Thermally sensitive
  - How to deal with this?
  - Isolated routing chip? Tuning?
  - What about 3D ICs? We want integration
- Current Art: Active tuning
  - Power cost of microheaters, *coarse* tuning
  - P-i-N tuning, limits of voltage
  - Thermal gradients = per-device tuning
    - Space, energy, feedback circuitry
  - Unavoidable, but can we improve upon it?

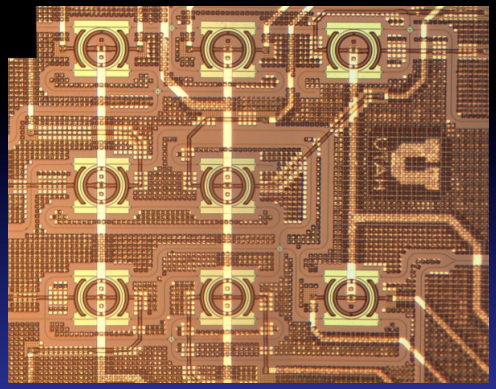


- Our Contribution:
  - Thermal-aware Resynthesis of Photonic Ring Resonators
  - Chip-level Thermal Characterization of Opto-Electronic Layouts

Our Silicon Photonics Full Adder Design

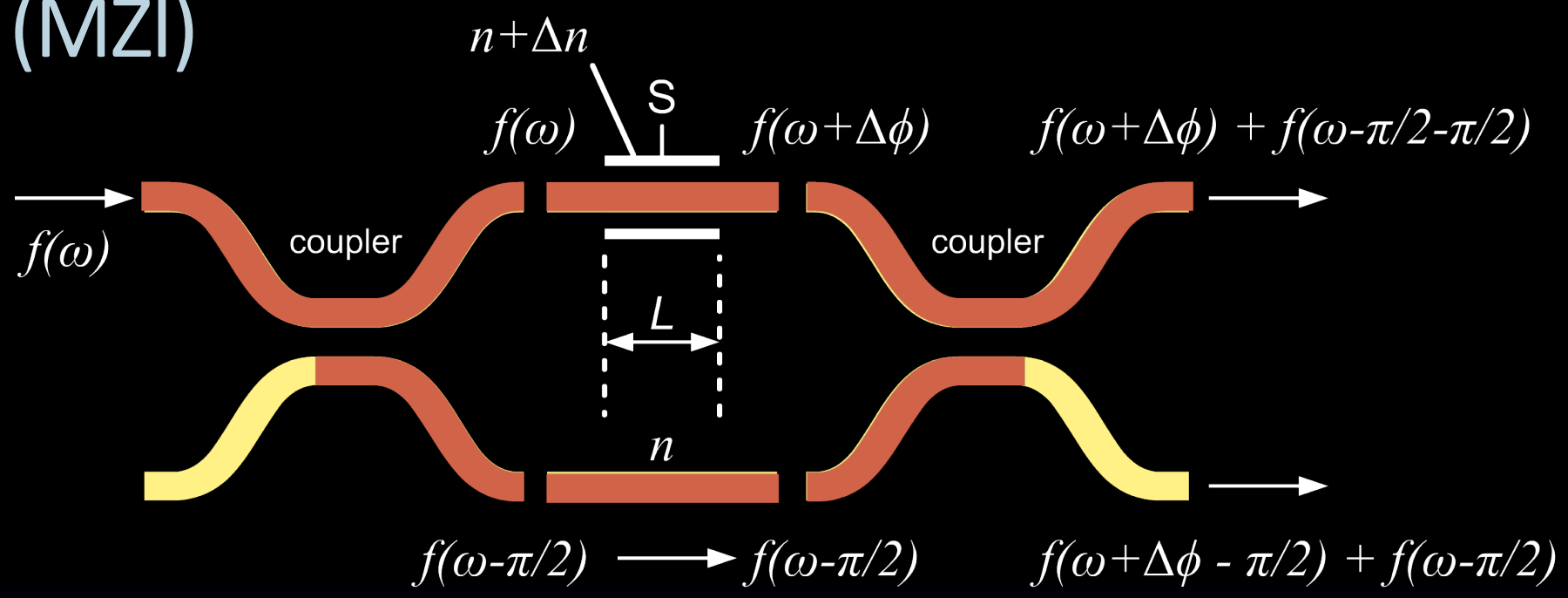






Fabricated using OpSIS

Switch: Mach-Zehnder Interferometer (MZI)

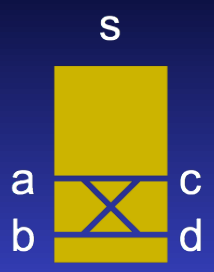


$$\phi_1 = \frac{\omega}{c} \cdot n \cdot L$$

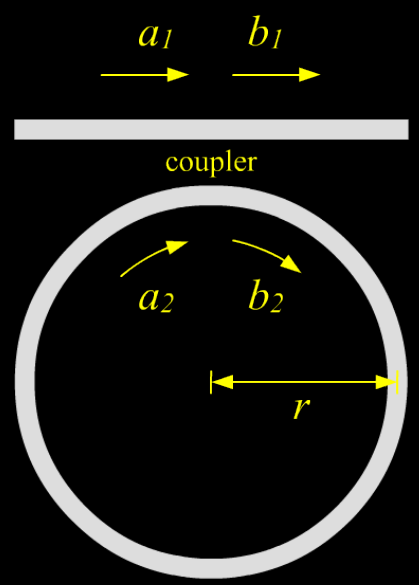
$$\phi_2 = \frac{\omega}{c} \cdot (n+\Delta n) \cdot L$$

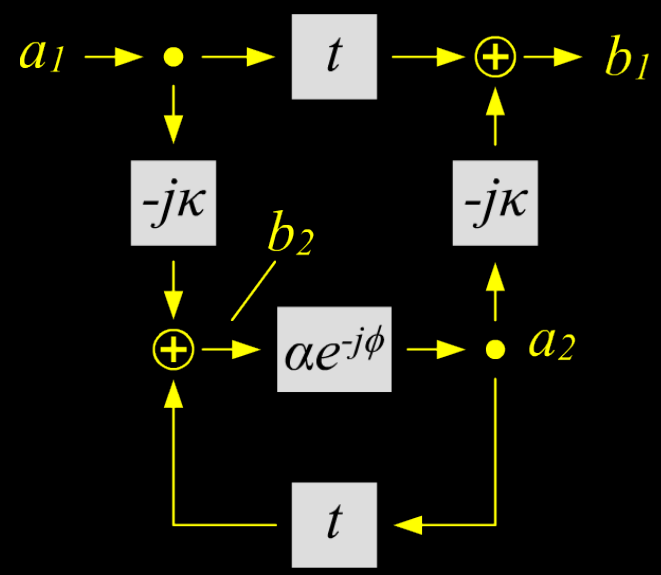
$$\Delta\phi = |\phi_2 - \phi_1| = \pi = \frac{\omega}{c} \cdot \Delta n \cdot L$$

S = 0 → Δϕ = π → bar
S = 1 → Δϕ = 0 → cross



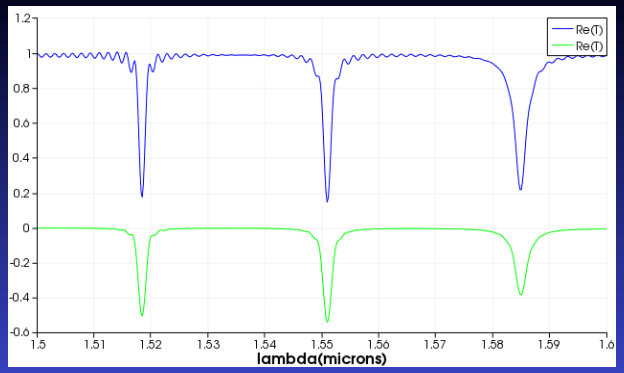
Switch: Optical Ring Resonators





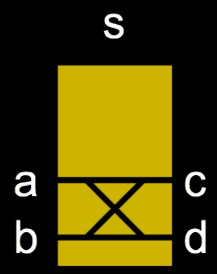
$$\frac{P_{b_1}}{P_{a_1}} = \left|\frac{E_{b_1}}{E_{a_1}}\right|^2 = \frac{\alpha^2 + |t|^2 - 2\alpha|t|\cos(\phi)}{1 + \alpha^2|t|^2 - 2\alpha|t|\cos(\phi)}$$

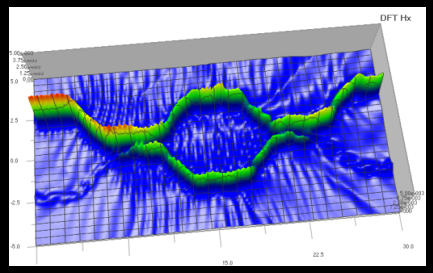
$$\phi = \beta \cdot L = \frac{2\pi n_{eff}}{\lambda_0} \cdot L = 2\pi \cdot m$$



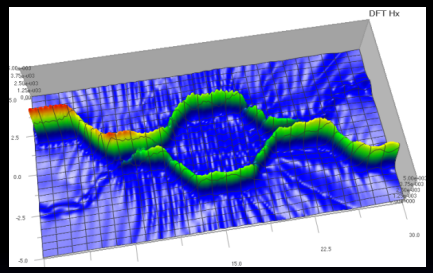
Crossbar Gates – Logic Building Block

- Electrically controlled 2x2 Optical Router ("switch")
  - s = *electrical* primary input
  - a, b, c, d = *optical* waveguides





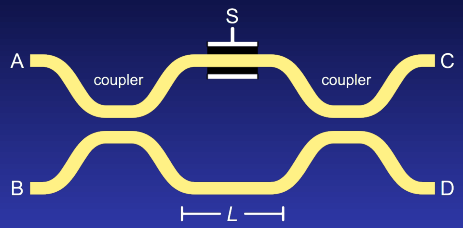
S = 0



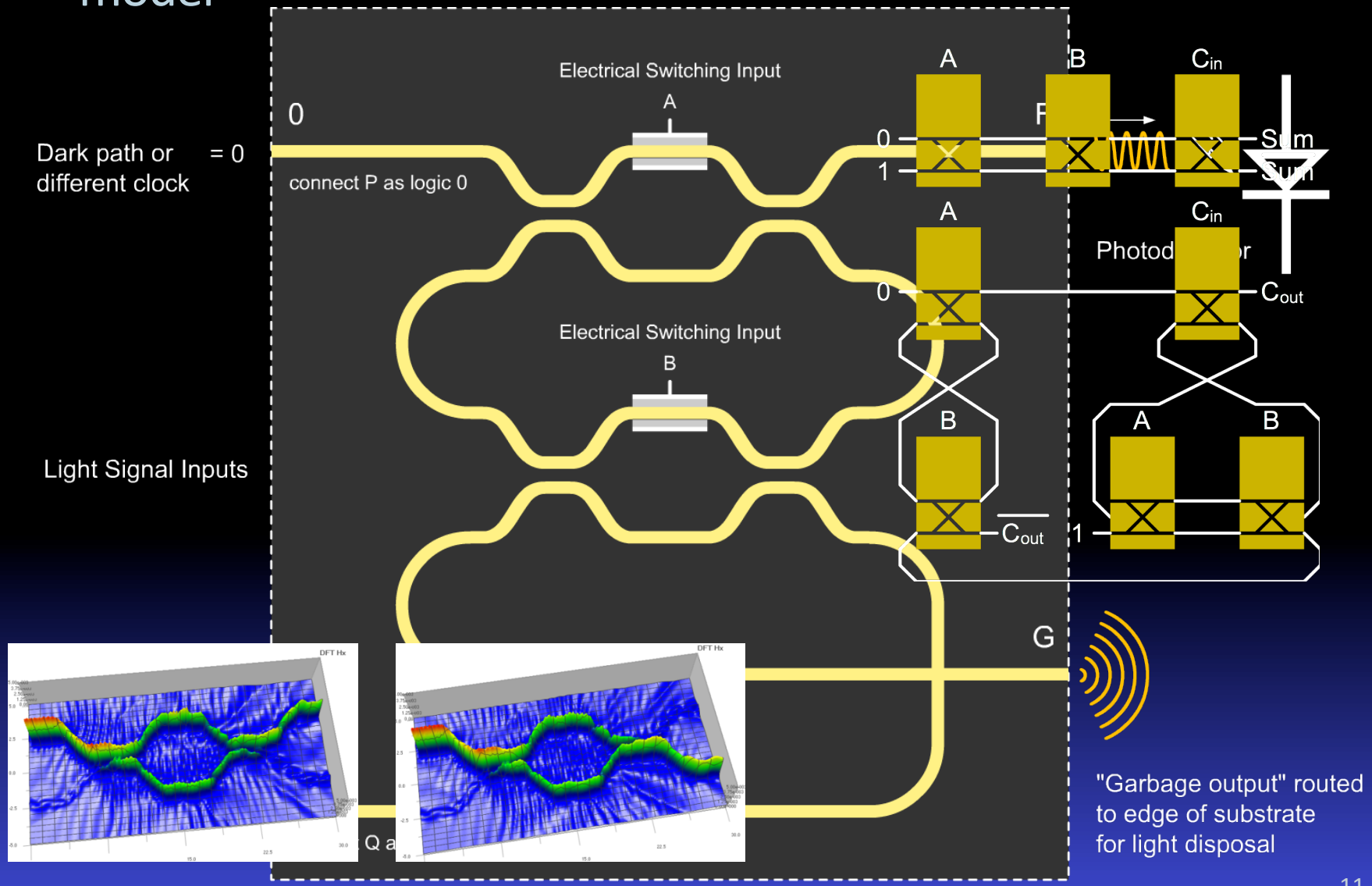
S = 1

- Crossbar Gate
  - S = 0 (bar) → (a = c, b = d)
  - S = 1 (cross) → (a = d, b = c)

- Switching devices
  - Mach-Zehnder Interferometer (MZI), ring resonators, MMIs, etc.

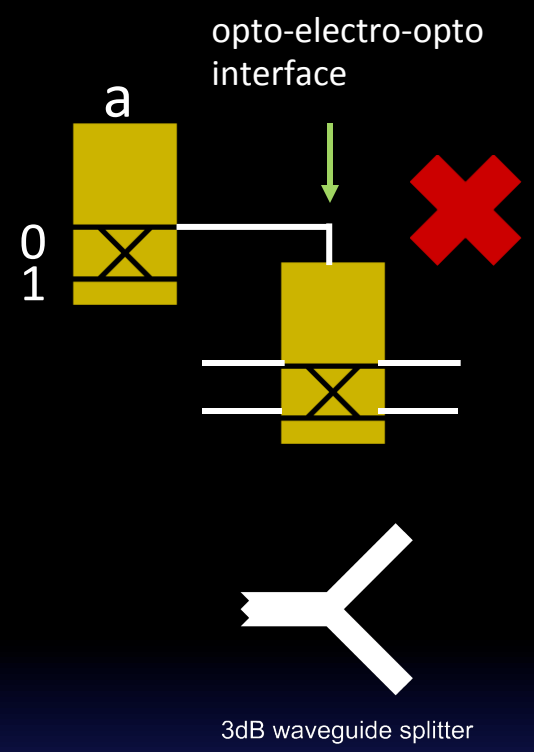


Logic Synthesis: Discrete component system integration model

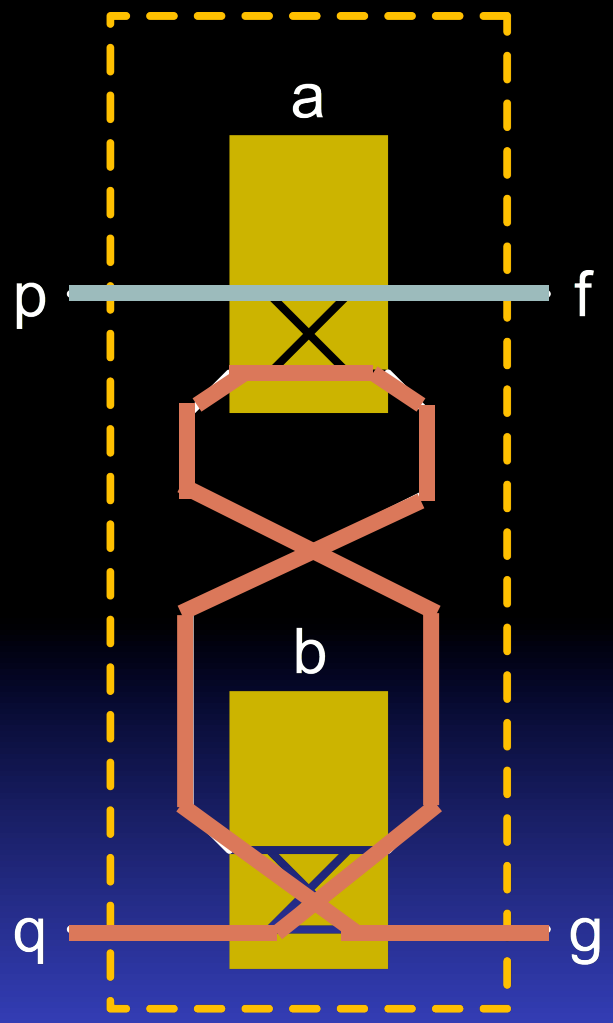


Technology Constraint Model

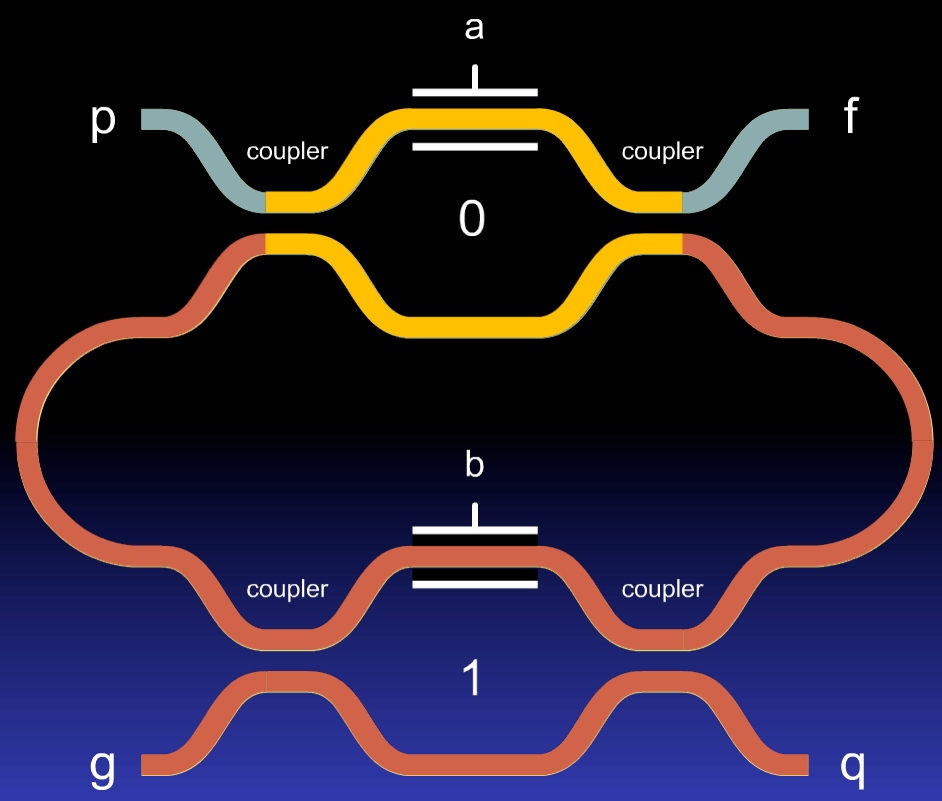
- Multi-level logic
  - Common sub-expression sharing
  - f: $B^n \rightarrow B^m$
  - Sis type factorization doesn't work
- Electro-optic interfaces
  - No mixing of electrical and optical signals
  - Sharing function outputs only through *optical splitters*
- Must account for unused optical outputs
  - "Garbage outputs" can produce noise
  - Routed to edge of substrate / absorbed
- Minimize number of gates
  - Gates have insertion losses
  - Area, routing overhead



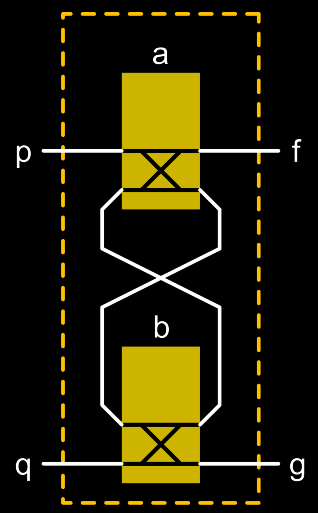
Virtual Gates



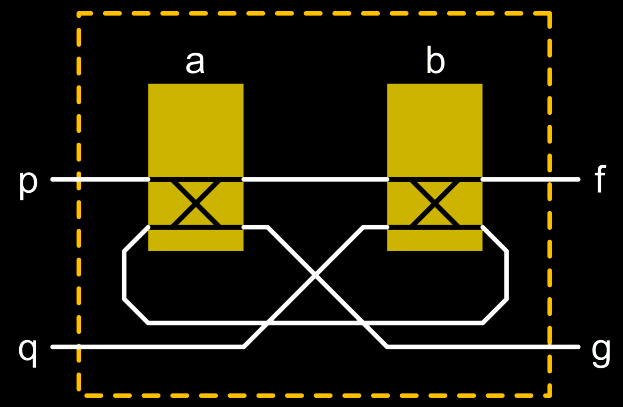
p = 0 q = 1 g = ¬ f



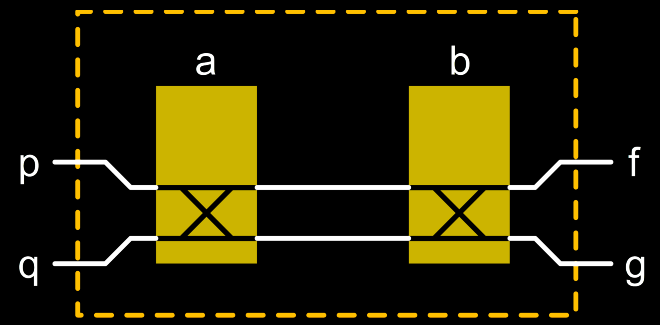
Virtual Gate Operators



AND



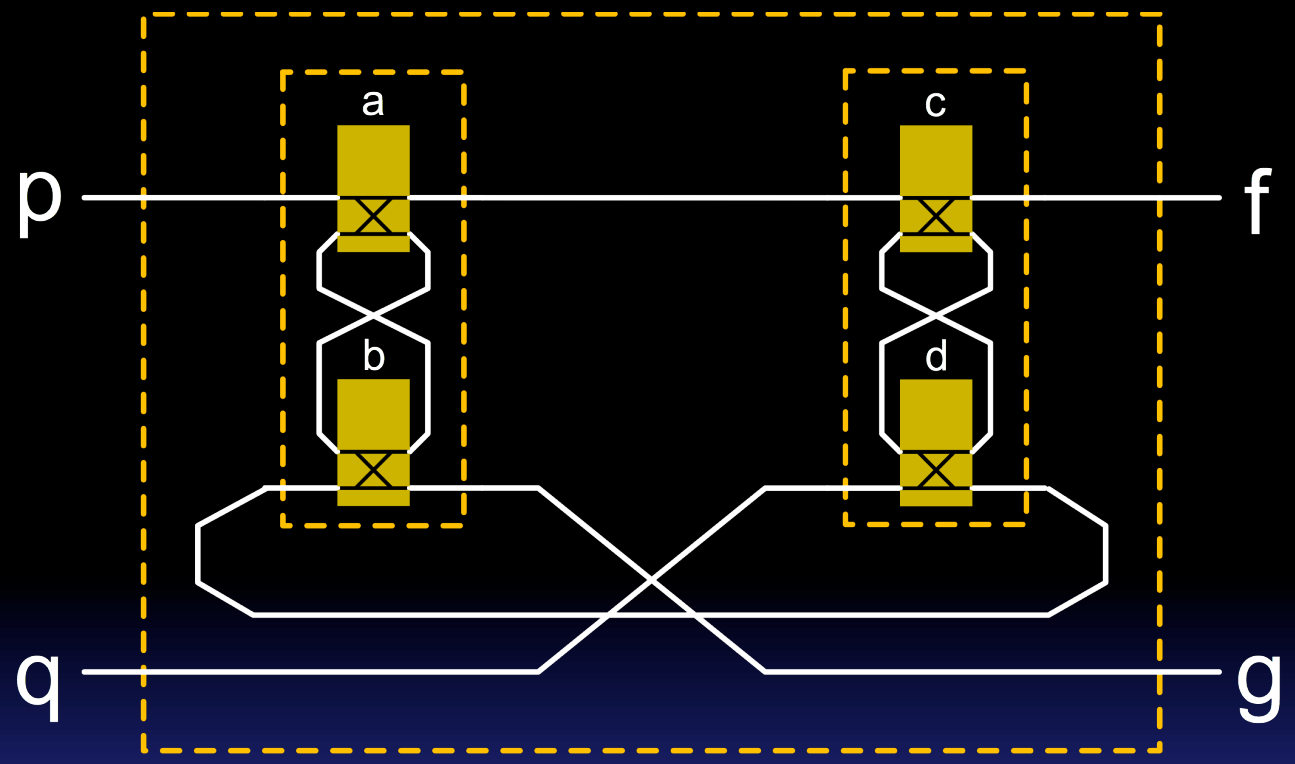
OR



XOR

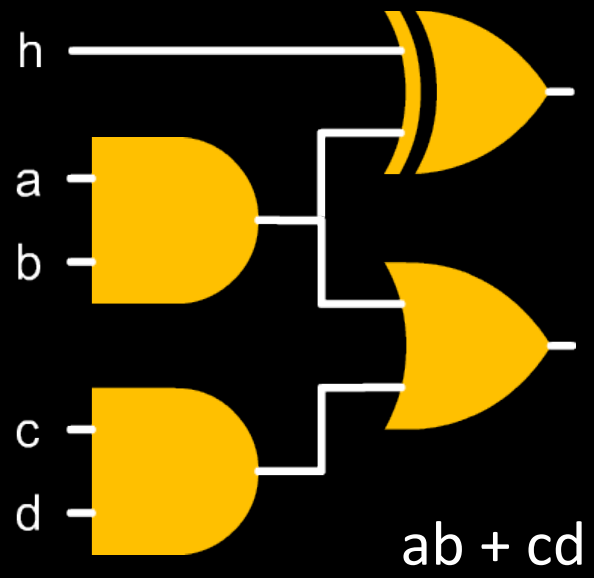
- Composition via “nesting”

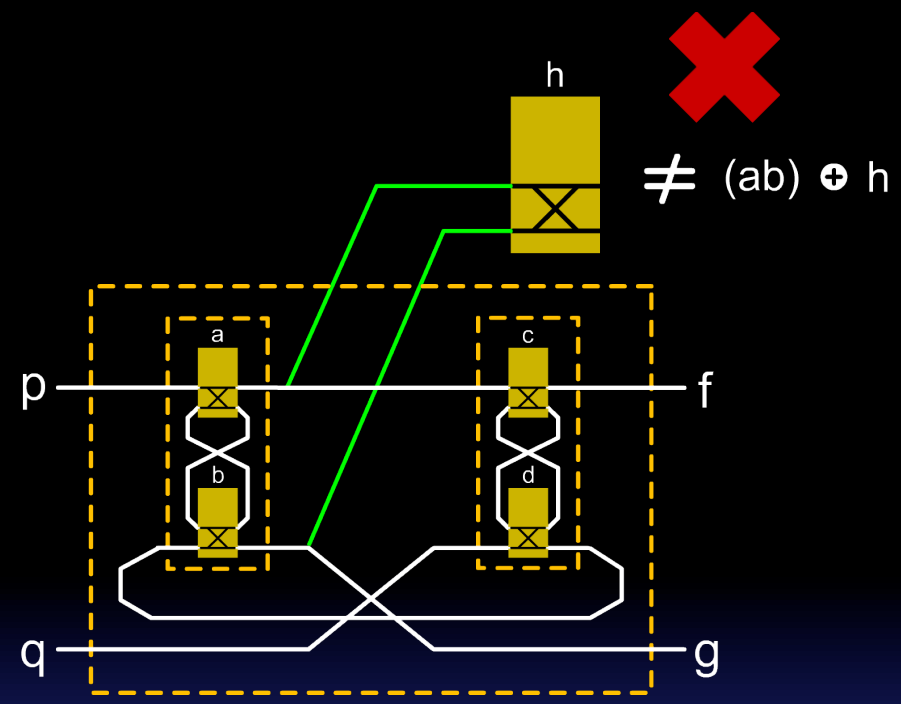
Composition: OR (AND (a, b), AND (c, d))



- How to share function outputs?

CMOS vs Optical Expression Sharing



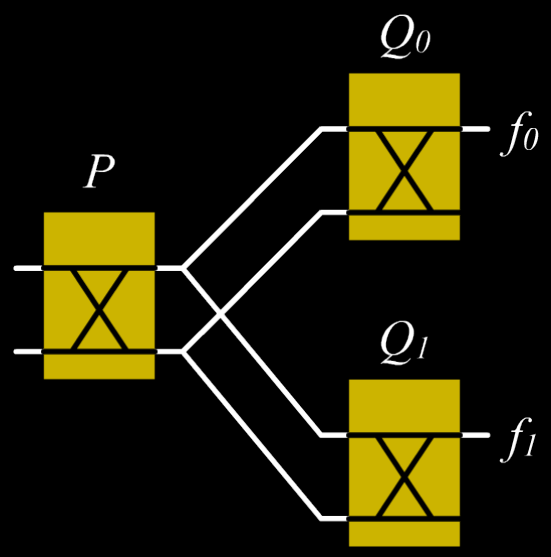


3dB waveguide splitter

Optical splitters only

Feedback loops prevent sharing

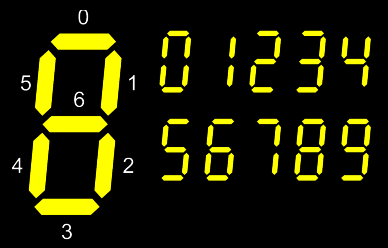
Expression Sharing Functions



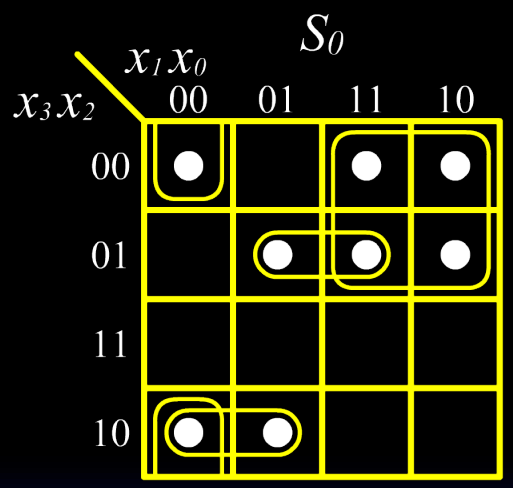
- Our Contribution
  - Hierarchical XOR-based CSE for Integrated Optics
- Objective
  - Reduce total number of literals in P, Q0, Q1
  - Move cubes between P, Q0, Q1 using XOR identity:
    - a ⊕ a = 0
- $f_0 = P \oplus Q_0$ $\quad$ $f_1 = P \oplus Q_1$

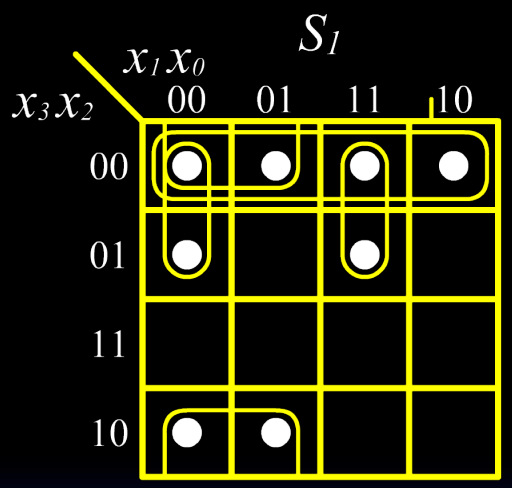
  $f_0 = (P \oplus m) \oplus (Q_0 \oplus m)$ $\quad$ $f_1 = (P \oplus m) \oplus (Q_1 \oplus m)$

BCD-to-7-segment



	$x_3x_2x_1x_0$	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1



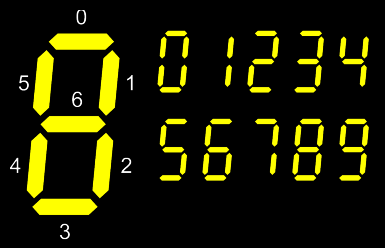


$$S_0 = \bar{x}_3 x_1 + \bar{x}_3 x_2 x_0 + \bar{x}_2 \bar{x}_1 \bar{x}_0 + x_3 \bar{x}_2 \bar{x}_1$$

$$S_1 = \bar{x}_3 \bar{x}_2 + \bar{x}_2 \bar{x}_1 + \bar{x}_3 \bar{x}_1 \bar{x}_0 + \bar{x}_3 x_1 x_0$$

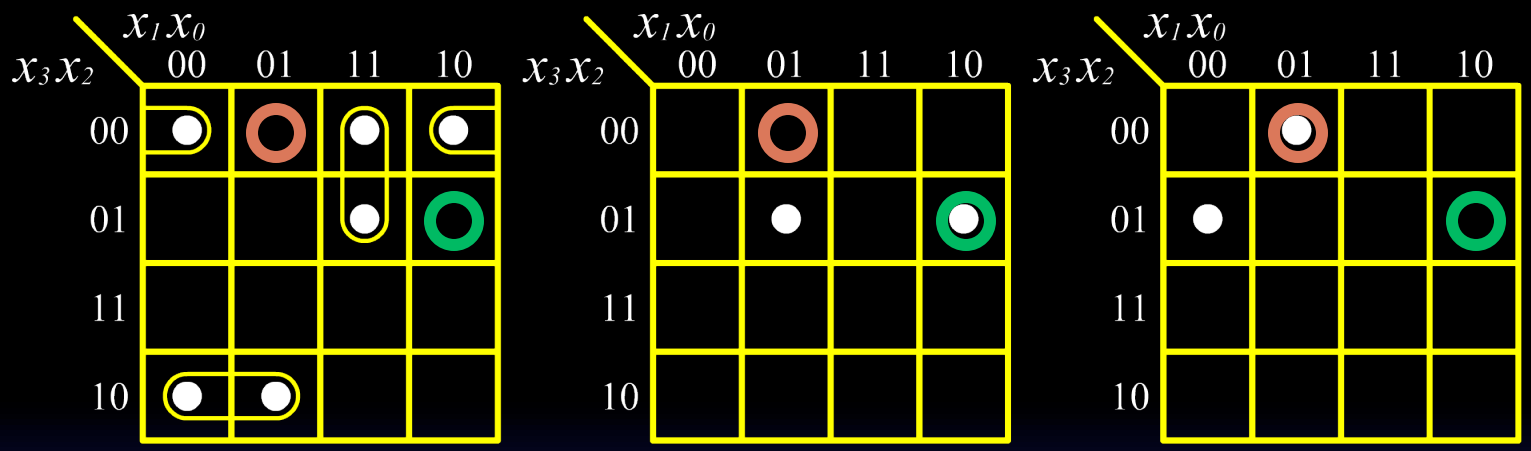
- 21 literals

BCD-to-7-segment



	$x_3x_2x_1x_0$	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1

- $P = S_0 \cdot S_1$ $\quad Q_0 = P \oplus S_0$ $\quad Q_1 = P \oplus S_1$



$$P = \bar{x}_3\bar{x}_2\bar{x}_0 + \bar{x}_3x_1x_0 + x_3\bar{x}_2\bar{x}_1$$

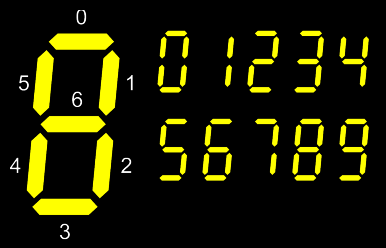
$$Q_0 = \bar{x}_3x_2\bar{x}_1x_0 + \bar{x}_3x_2x_1\bar{x}_0$$

$$Q_1 = \bar{x}_3\bar{x}_2\bar{x}_1x_0 + \bar{x}_3x_2\bar{x}_1\bar{x}_0$$

Objectives:

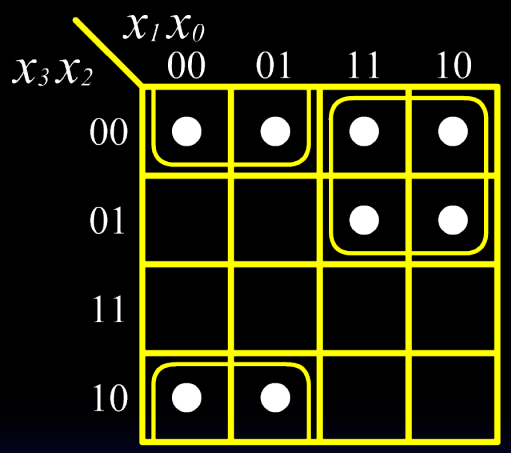
- Reduce total literal count by moving cubes to other functions.
- Find good “m” that will reduce total literal count

BCD-to-7-segment

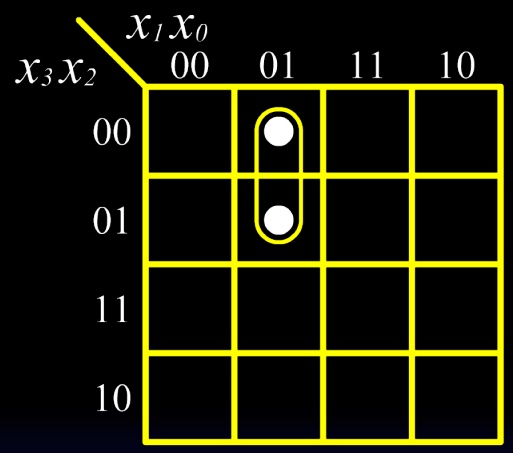


	$x_3x_2x_1x_0$	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1

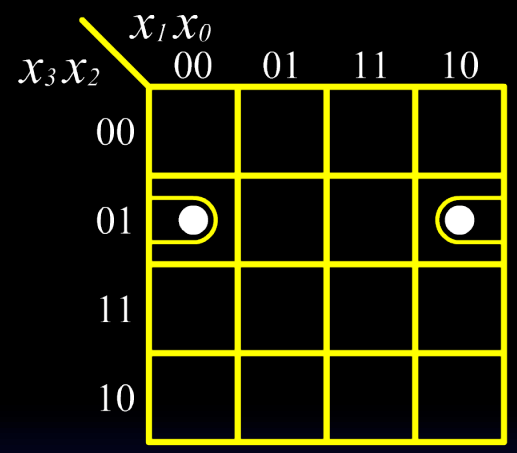
- $P = S_0 \cdot S_1$ $\quad Q_0 = P \oplus S_0$ $\quad Q_1 = P \oplus S_1$



$P = \bar{x}_2\bar{x}_1 + \bar{x}_3x_1$



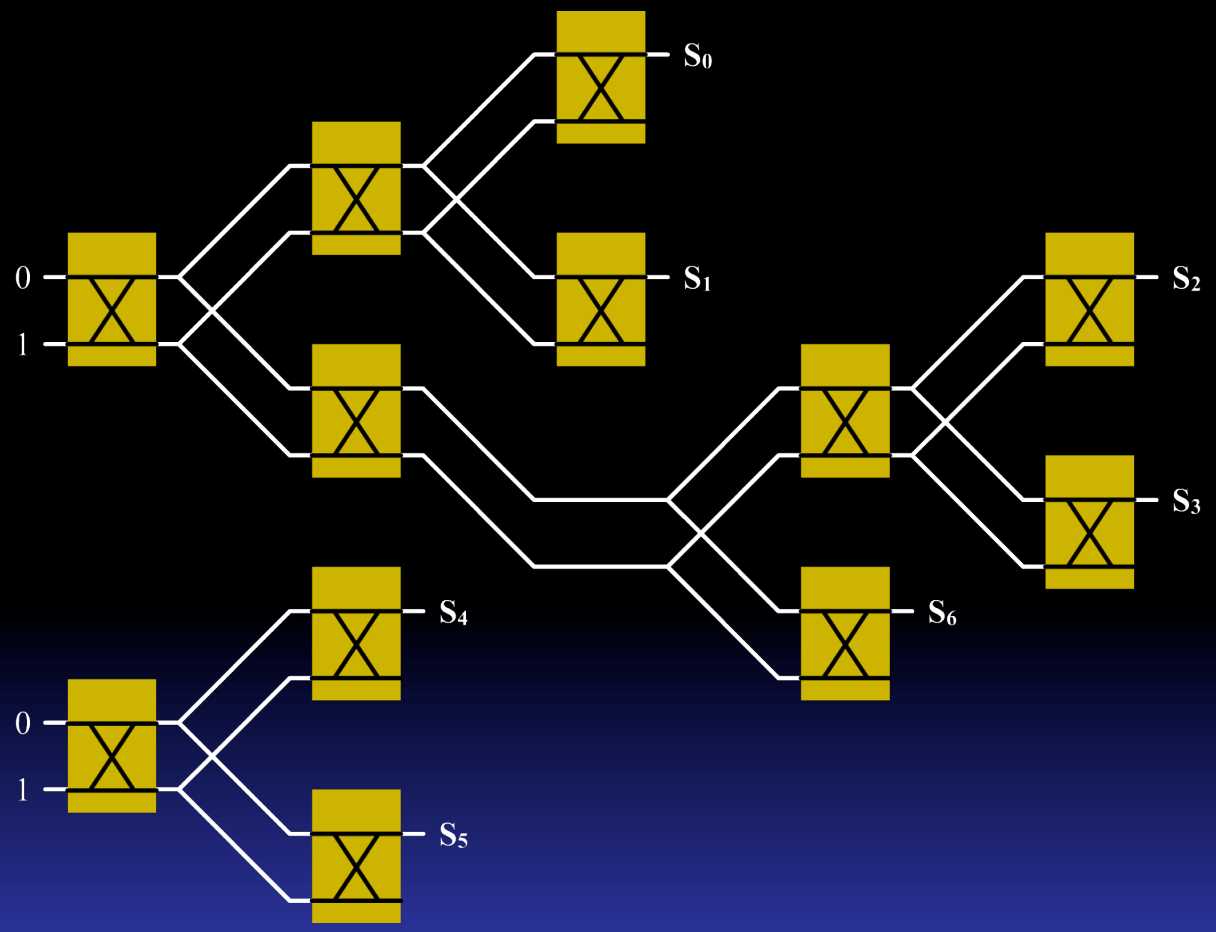
$Q_0 = \bar{x}_3\bar{x}_1x_0$



$Q_1 = \bar{x}_3x_2\bar{x}_0$

- 10 literals

Multi-level Logic Decomposition

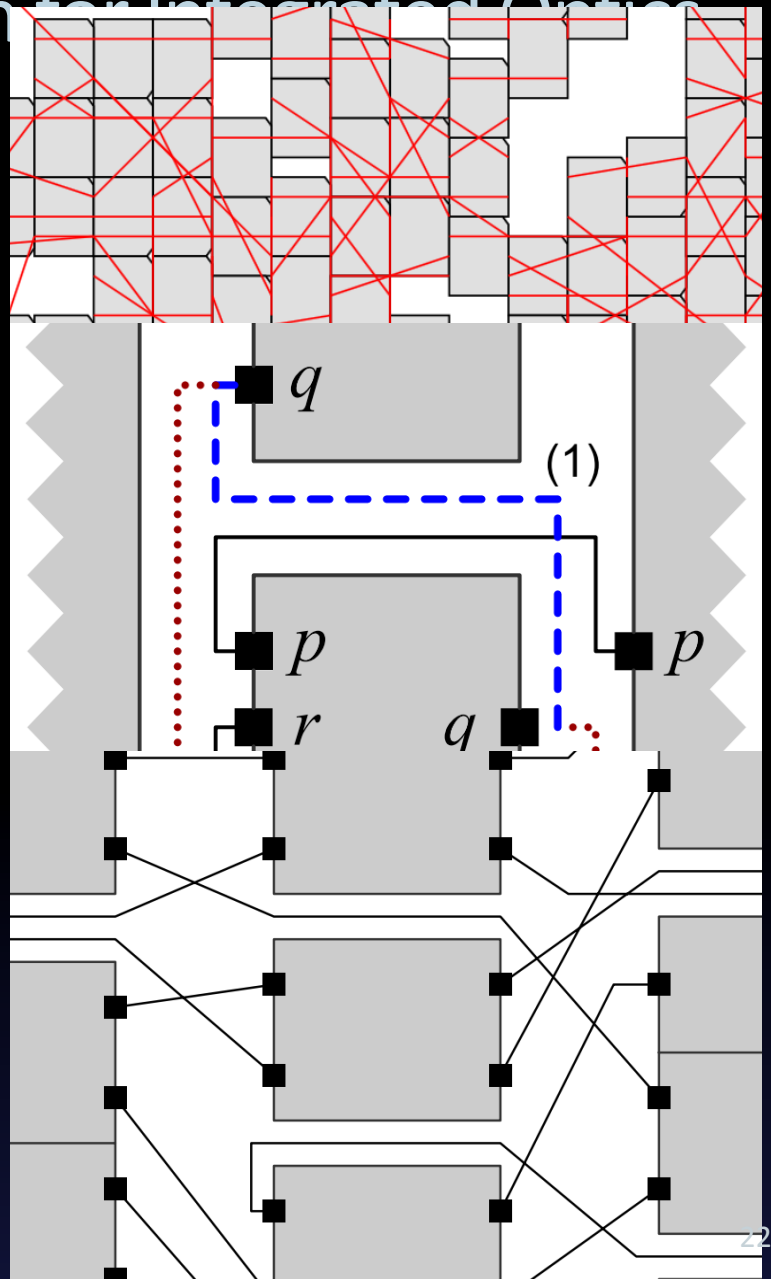


Physical Design Automation for Integrated Optics

Placement

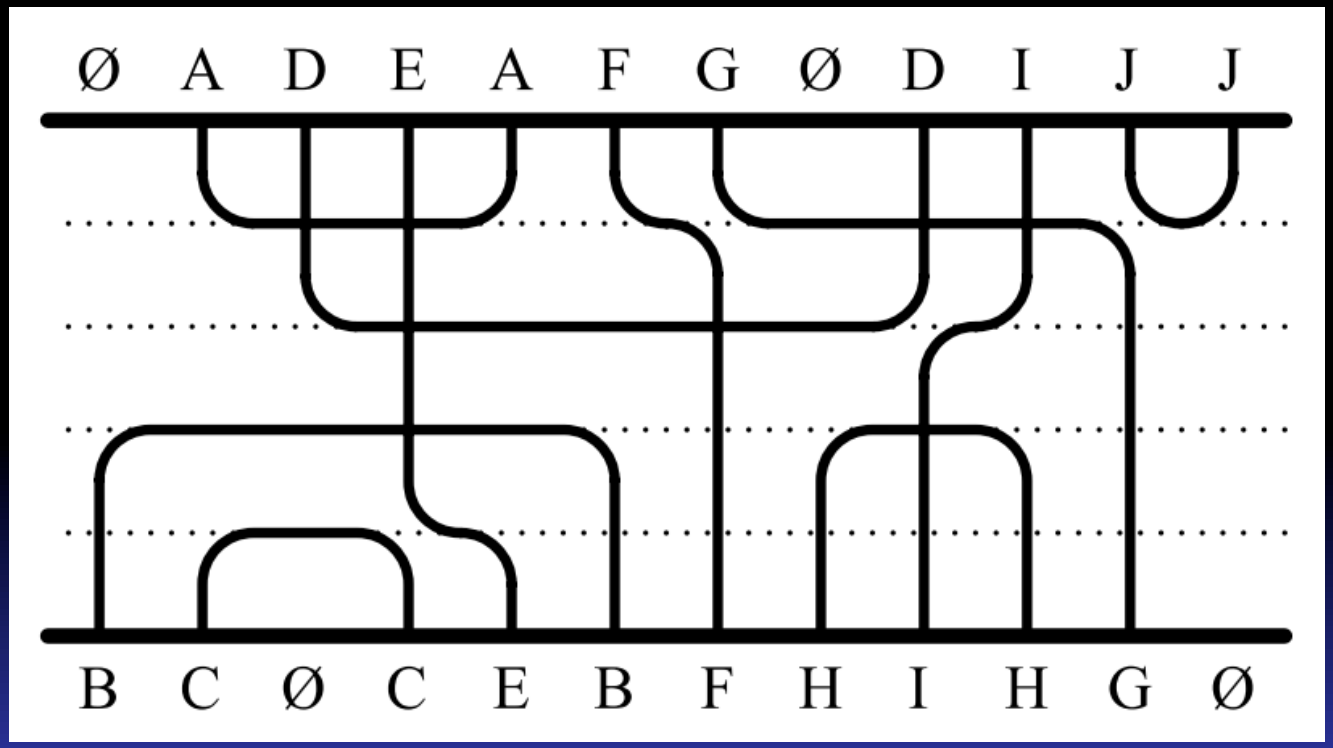
Global Routing

Channel Routing



Channel Routing for Waveguides

- Exploit Waveguide Profiles and Bends



Design Constraints – Signal Loss + Area

Crossings

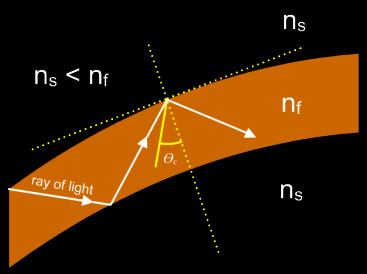
- 0.1-0.2 dB / crossing
- 5 – 10um in size

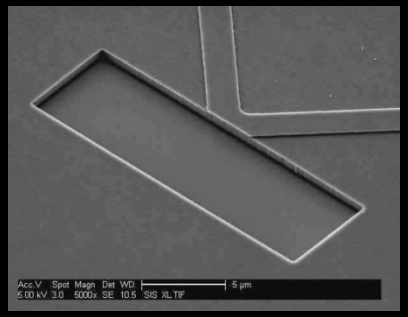
Bends

- dB / cm
- dB / bend
  (e.g. 0.1dB @ 1um;
  0.007dB @ 50um)
- < 1 – 10um+

Straight waveguides

- dB / cm
- ~0.5um width





Yusheng Qian, Jianhua Jiang, et al
Electrical and Computer Engineering,
Brigham Young University;
Nano and Micro Devices Center,
University of Alabama in Huntsville

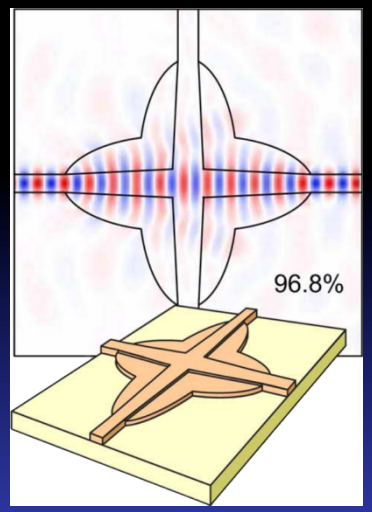
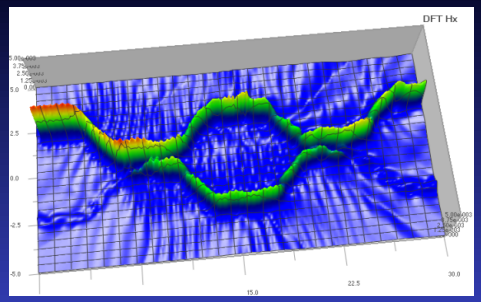


Image credit: Bogaerts et al



Channel Routing

Minimize signal loss

- Crossings
- Bends

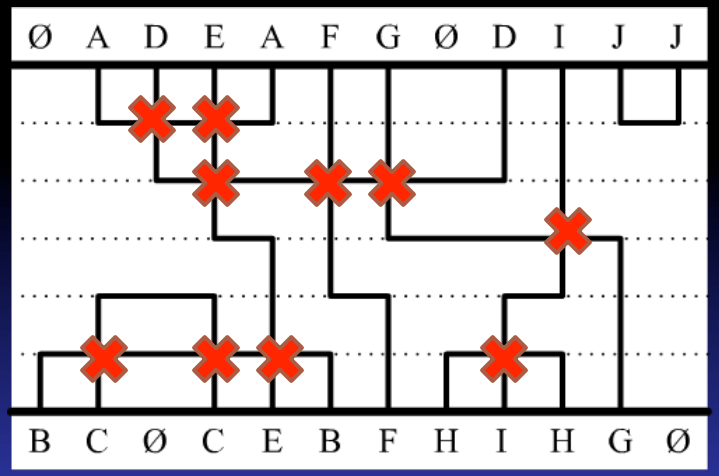
Track minimization

Swap-based

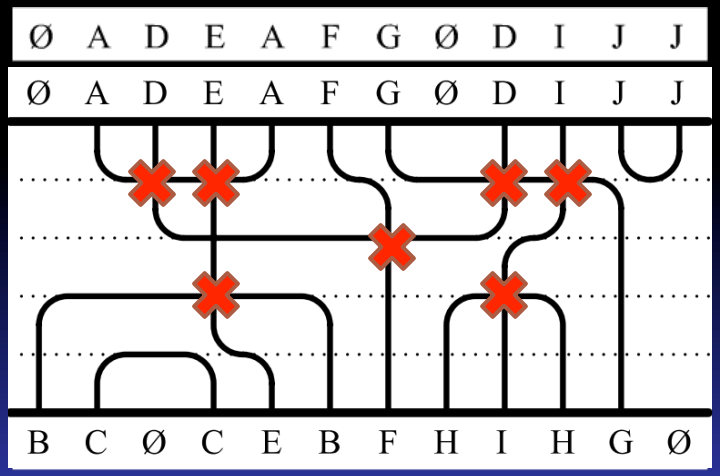
- Octilinear grid
- 2-sided sorting

Left-edge/YK style

- Constraints to graph
- Knock-knee extension



10 crossings

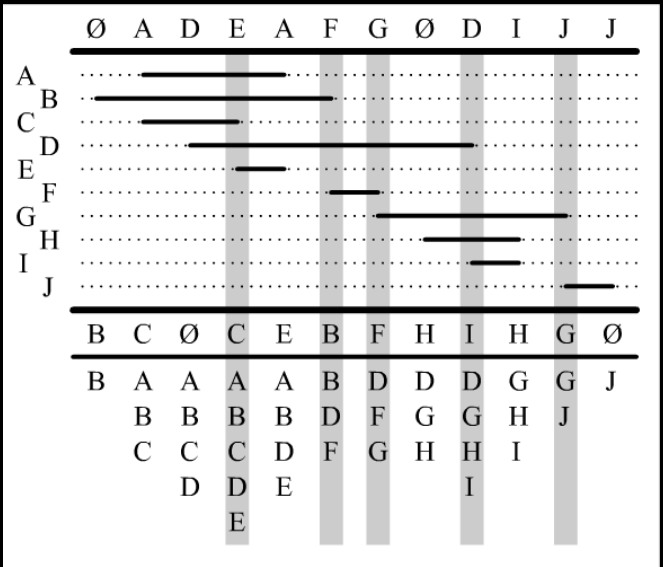


8 crossings

Conventional Left-Edge/VLSI Channel Routing

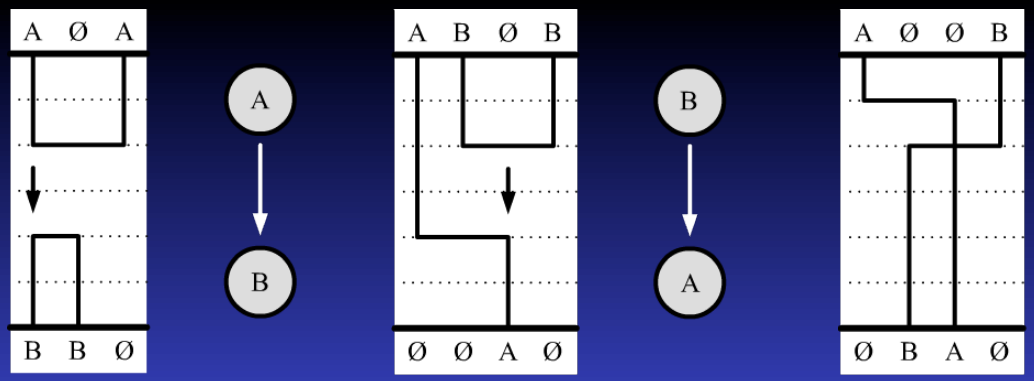
Horizontal constraint graph

- Zone representation
- Horizontal overlap

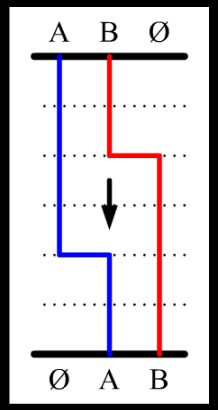


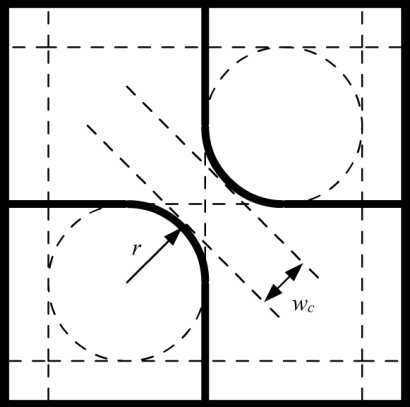
Vertical constraint graph

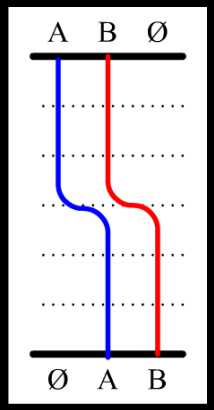
- End-spans
- Crossing avoidance

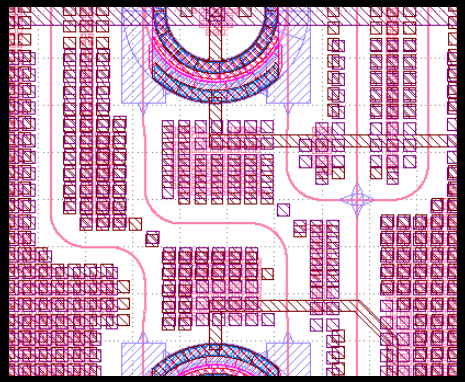


Knock-knee Extension



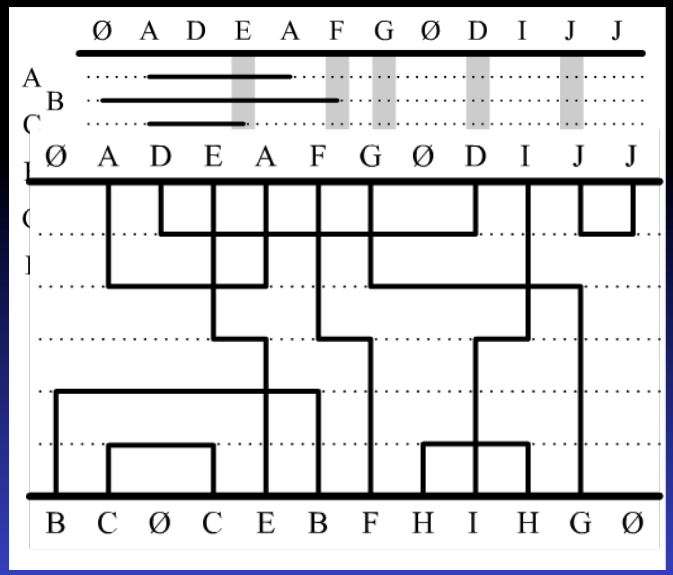


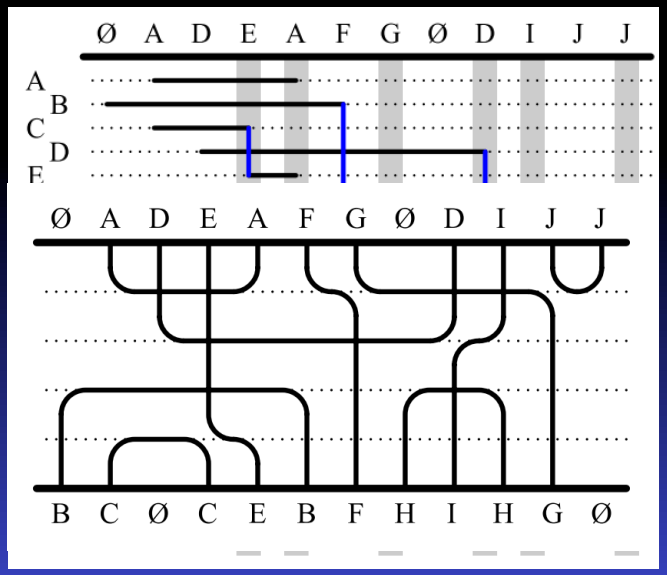




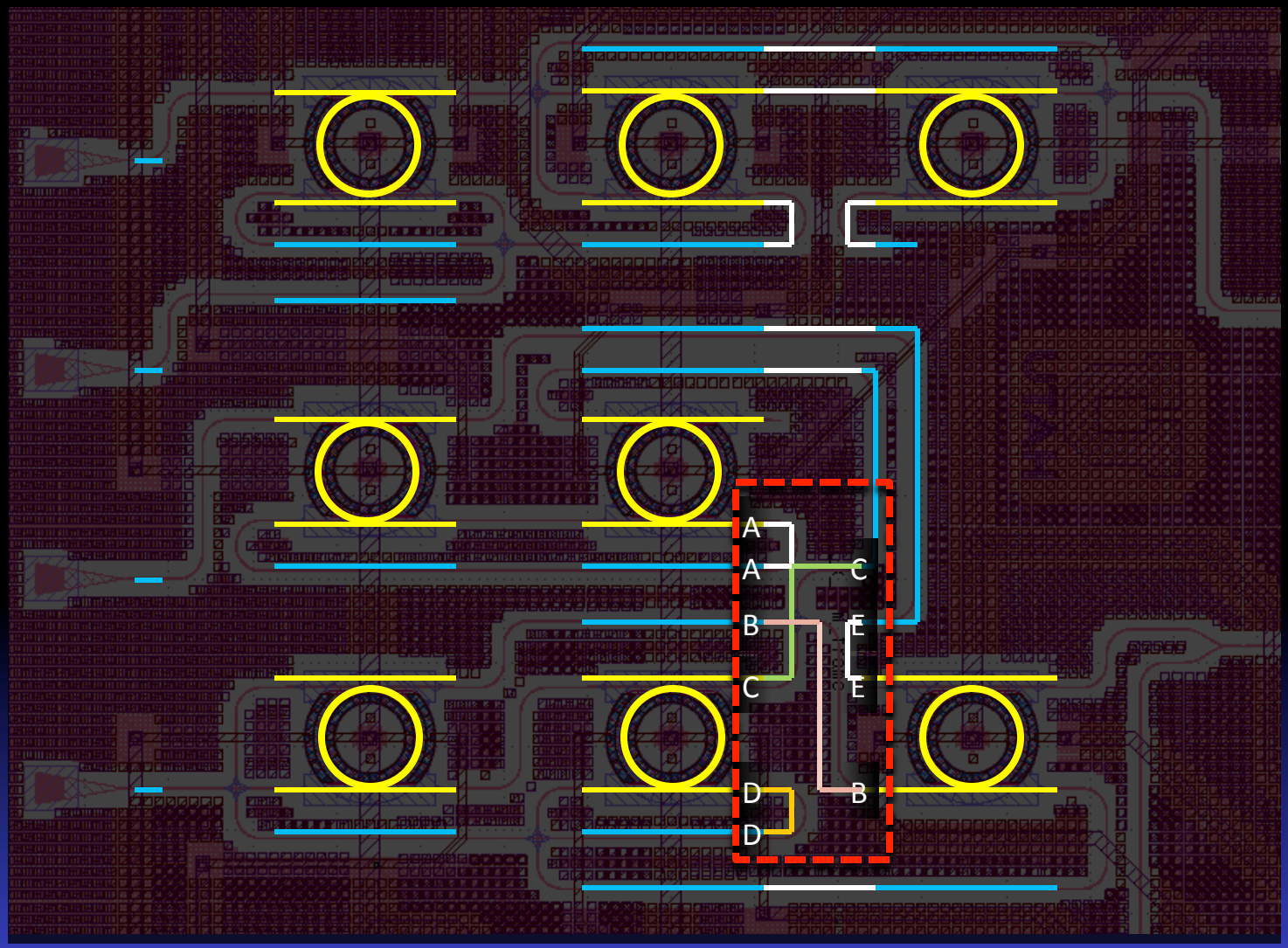
2 tracks

1 track

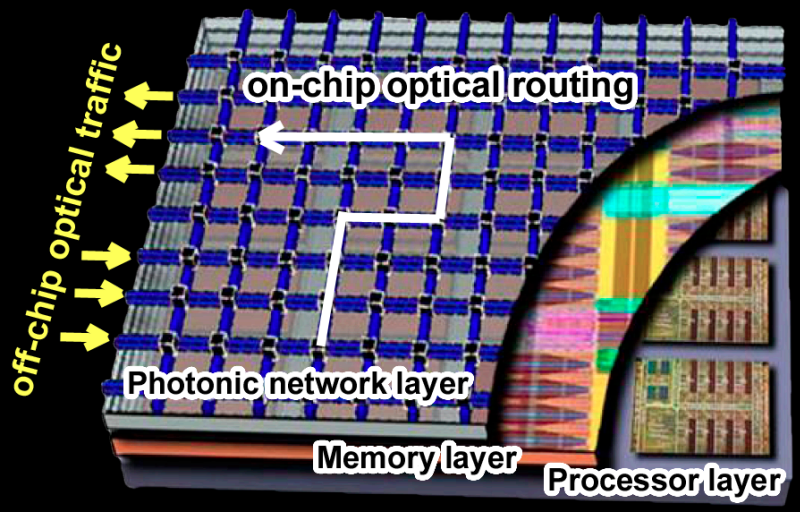


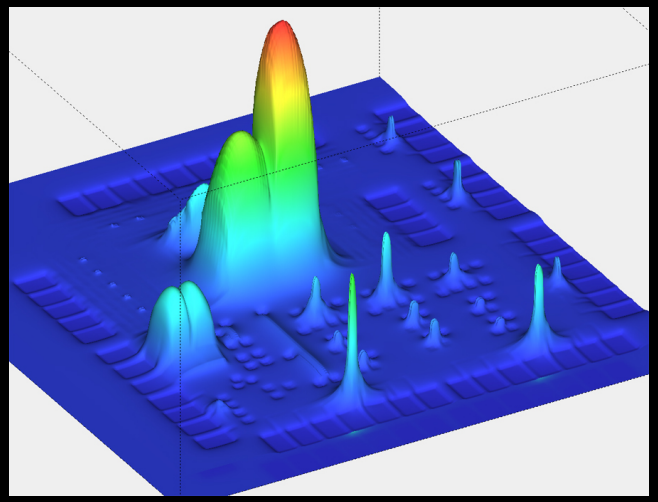


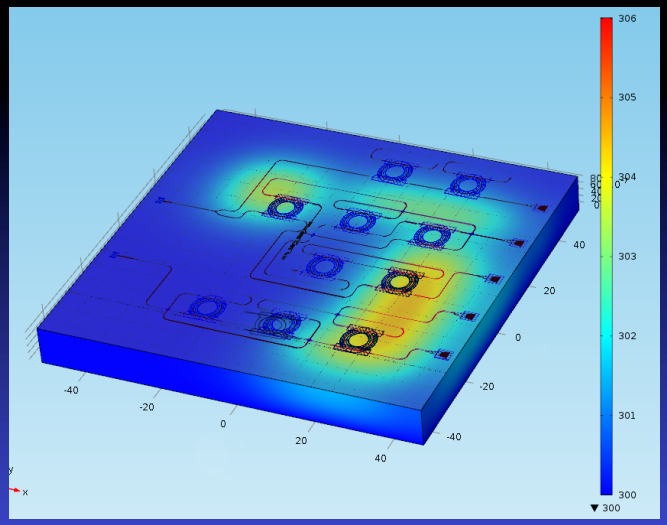
Physical Synthesis on a Real Design



Optical NoCs: Thermal Gradients

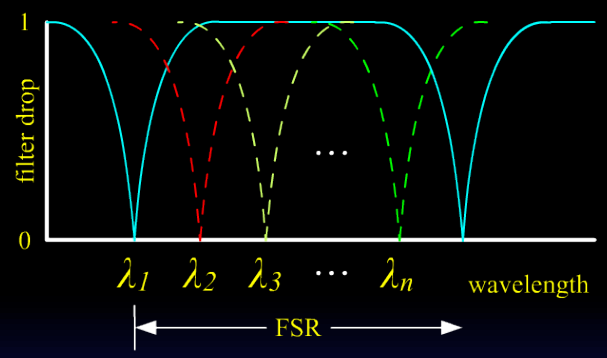


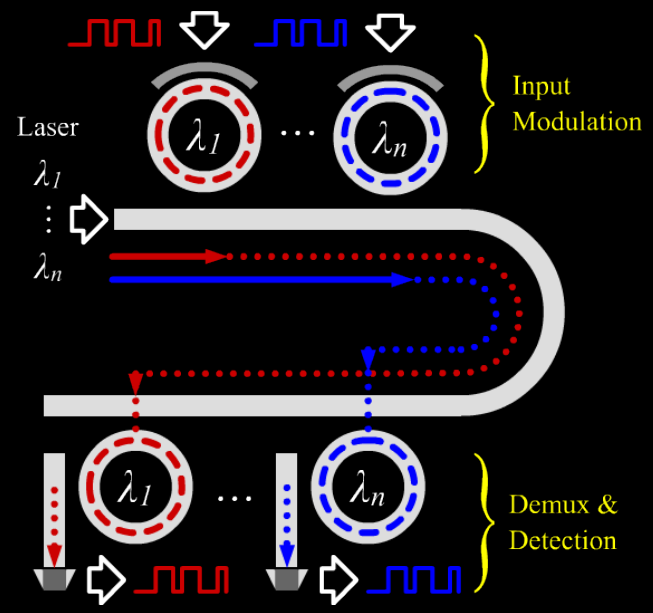




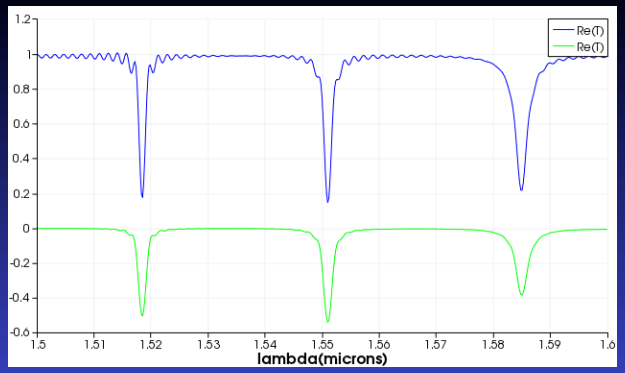
Thermal-aware Resynthesis

- WDM networks
  - Multiple channels
  - Multiple wavelengths

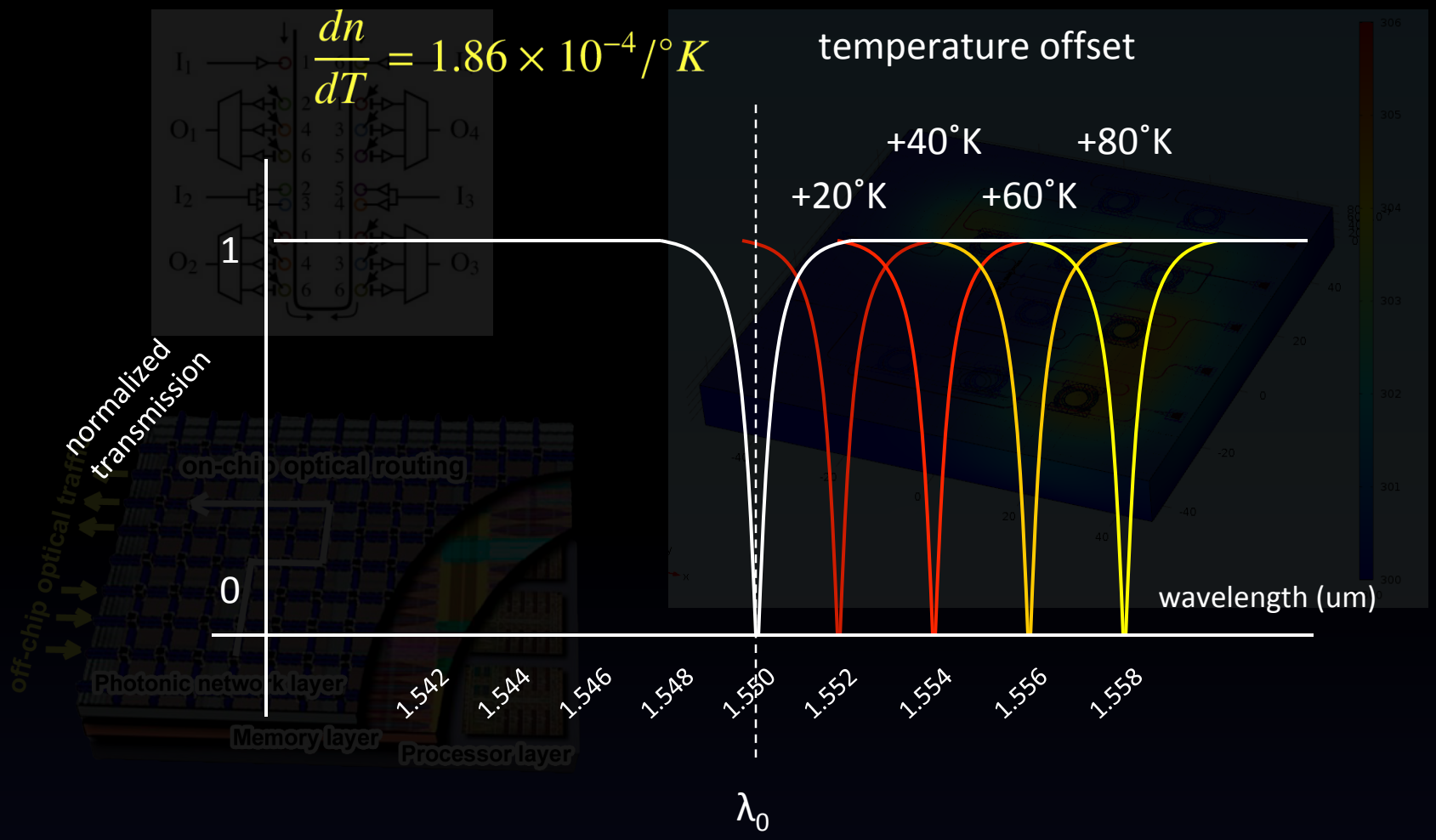




- Mux/Demux
  - Ring resonator



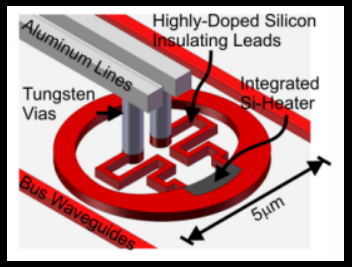
System Integration and Thermal Gradients



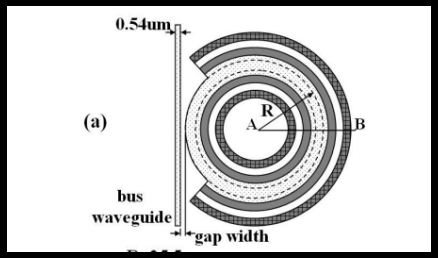
Thermal Compensation

- Active Tuning
  - Microheaters
    - Coarse grained
    - *Adding* heat to system
    - Shifting to bring it back (periodic)
  - P-i-N biasing
    - Fine grained, small range
    - Limits to voltage
- Architectural
  - Sub-channel remapping
    - Area, channel overlap
  - Avoidance
- Athermal Design
  - Polymers hybrids

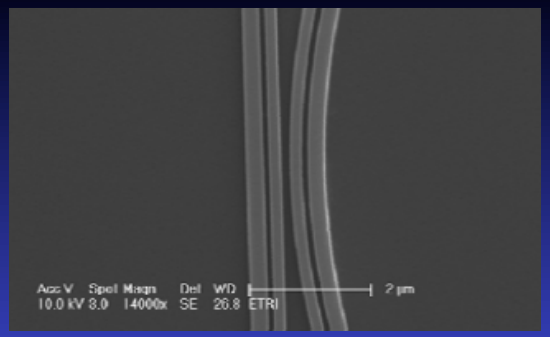
- Active Tuning Is Unavoidable
  - Complement active tuning
  - *Static compensation to reduce power*



"Adiabatic Resonant Microrings (ARMs) with directly integrated thermal microphotonics", *M. Watts, et al., OSA 2009*

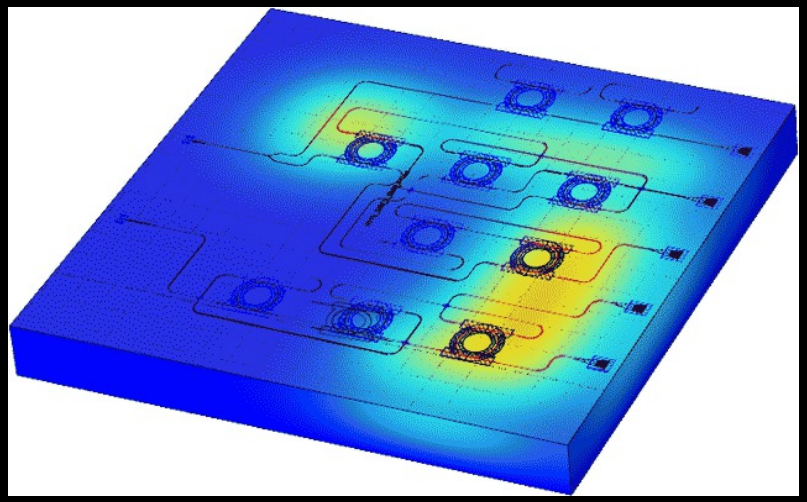


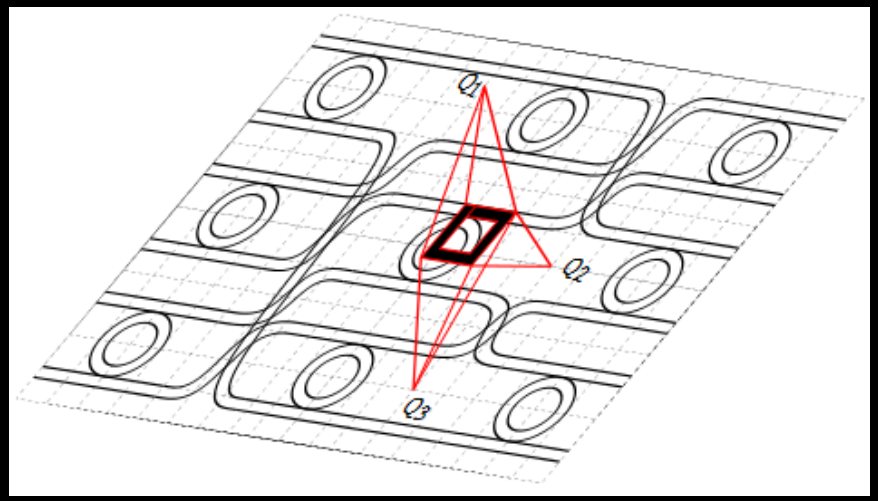
"Extinction ratio compensation by free carrier injection for a MOS-capacitor microring optical modulator subjected to temperature drifting", *C. T. Shih, et al., CLEO 2009*



"Controlling temperature dependence of silicon waveguide using slot structure", *J-M Lee et al, Opt Exp. 2008*

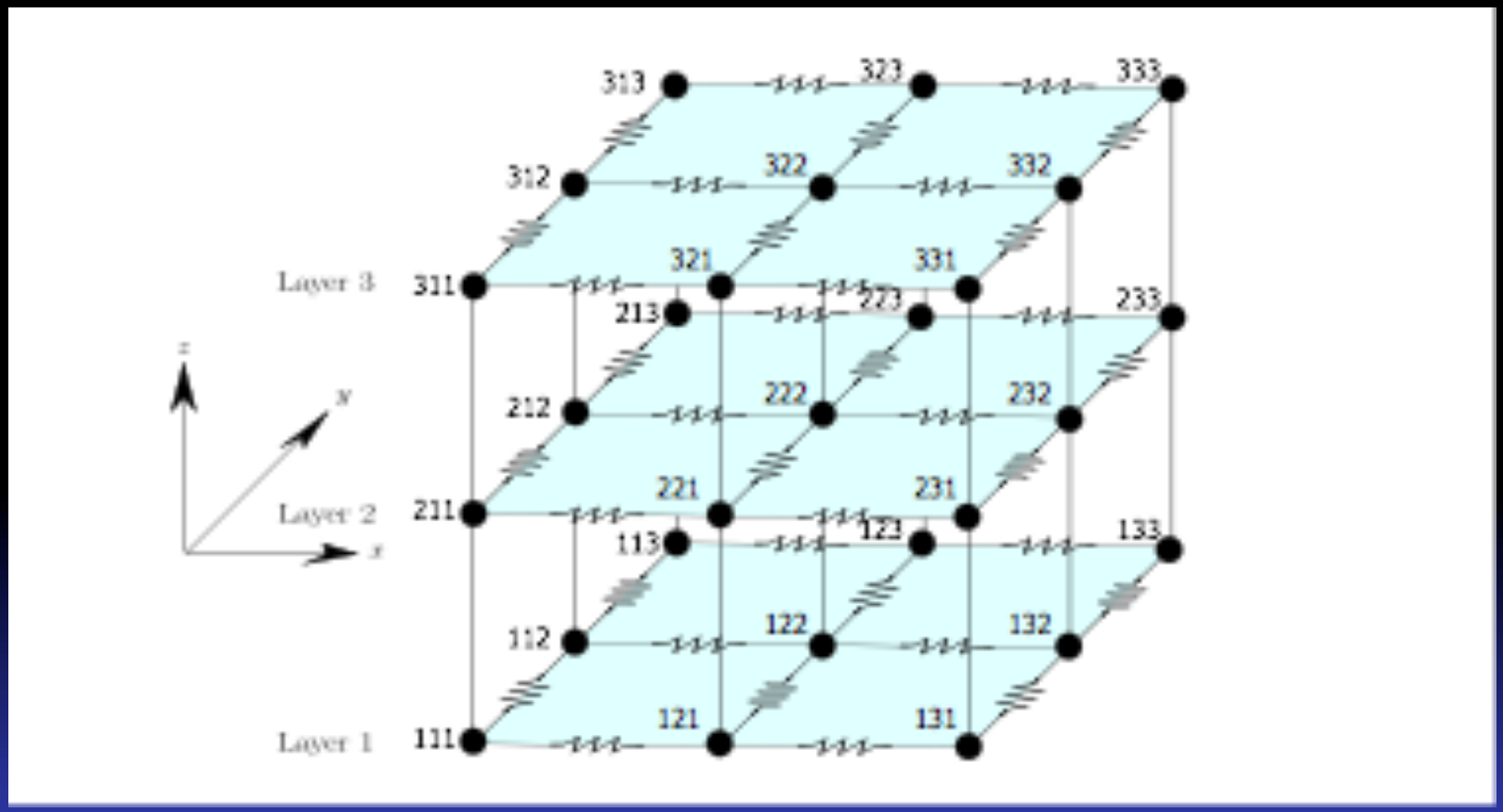
Thermal Gradient Abstraction



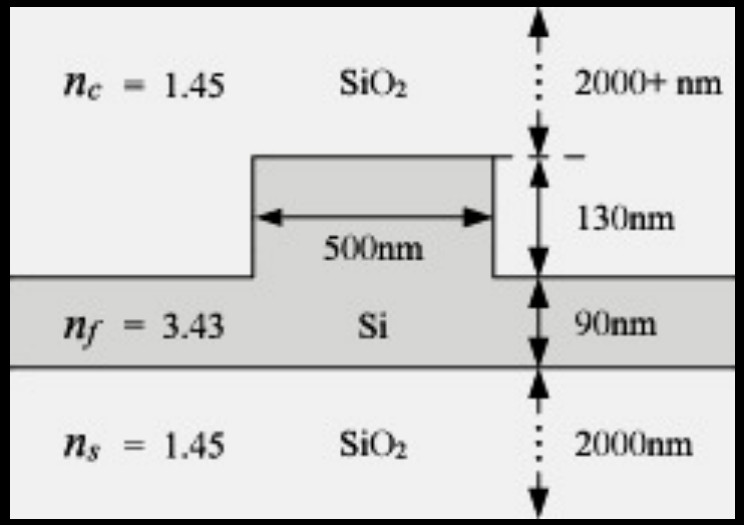


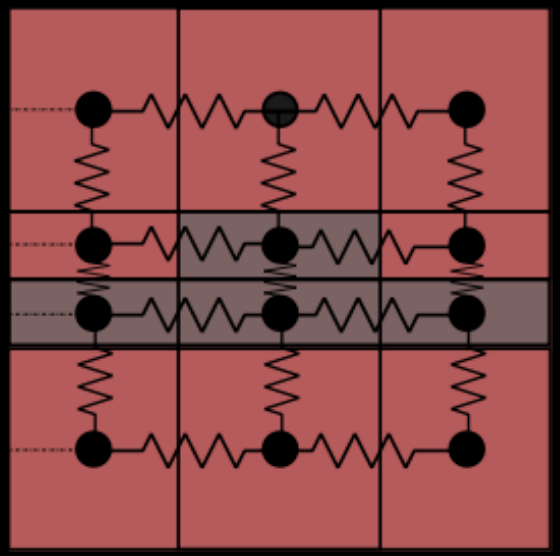
- Simulate hot-spots, compute thermal gradient
- Break Ring into Segments $L=2\cdot\pi r=\sum L_i$
- Estimate $\eta_{eff}=\sum_i n_i\cdot L_i/L$

Finite Difference Discretization



Naturally non-uniform Discretization





- Analyze the layout, layer-by-layer
- Thermal resistance model, solved 7-point FDM
- Estimate phase change in every ring
- Unlike VLSI, optical layouts are sparser

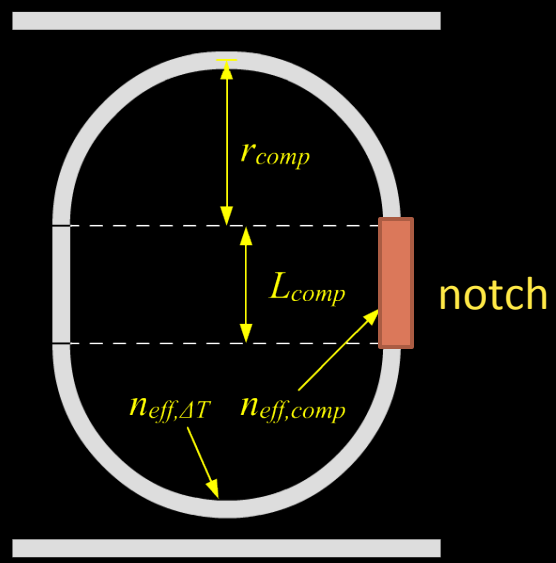
Design space exploration

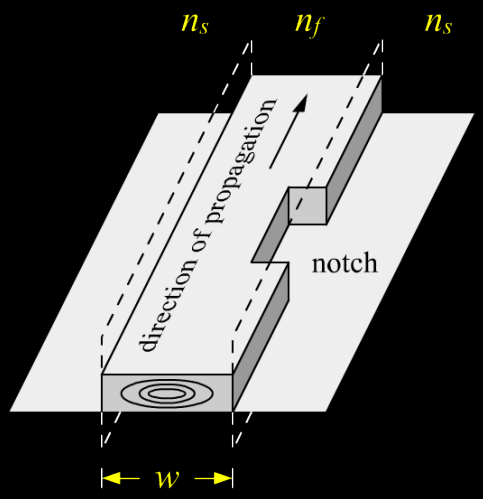
- Static compensation
  - Satisfy Resonant Condition

$$\phi = \beta \cdot L = \frac{2\pi n_{eff}}{\lambda_0} \cdot L = 2\pi \cdot m$$

  - Resynthesize ring resonators using 2D structure changes:
    - Ring length
    - Waveguide width

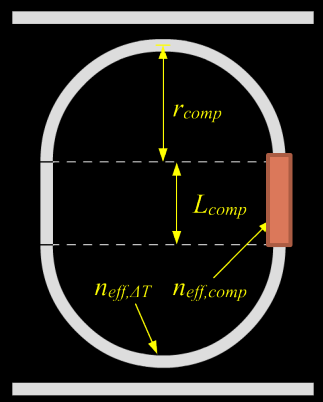
Compensation using Notch Width

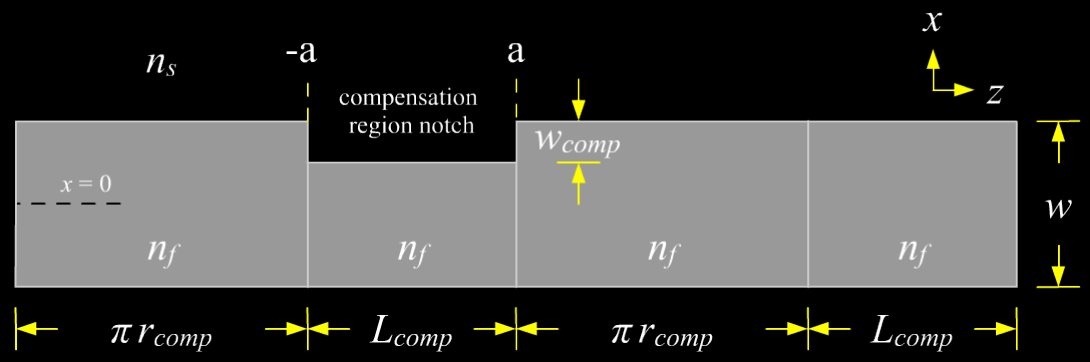




$$\phi = 2\pi m = \int_0^L \beta(z)dz$$
$$= \beta_{\Delta T}\left(2\pi r_{comp} + L_{comp}\right) + \beta_{comp}L_{comp}$$

Modeling Notches





$$E(z) = \frac{A^+(-a)}{2} e^{-j(\beta+\kappa)z} \qquad \text{for } -a < z < a$$

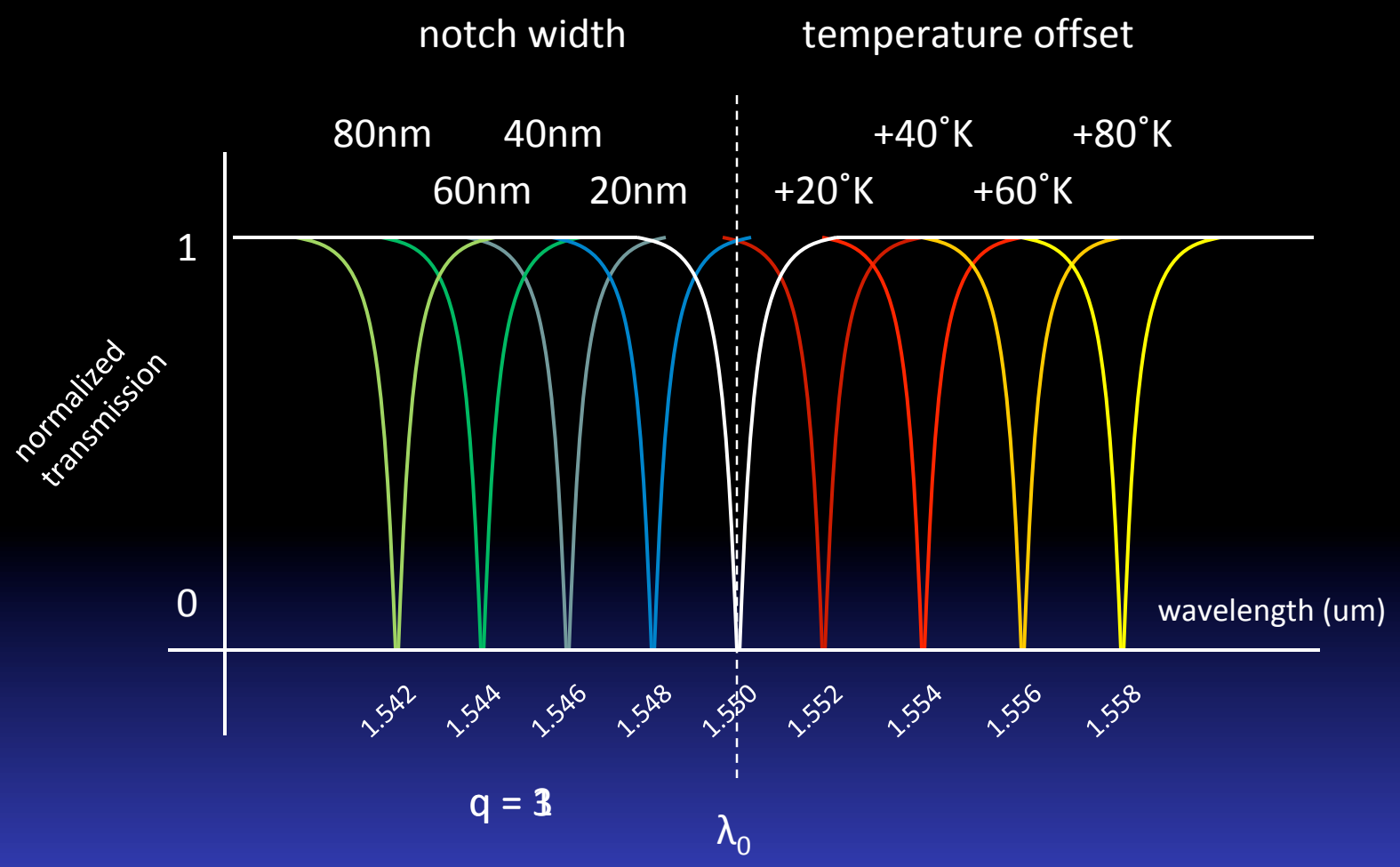
$$A^-(-a) = \frac{-j\kappa A^+}{\beta} \sin(2\beta a)$$

$$2\beta a = q\pi \qquad \Rightarrow \qquad a = \frac{q\pi}{2\beta} = \frac{\lambda}{4}$$

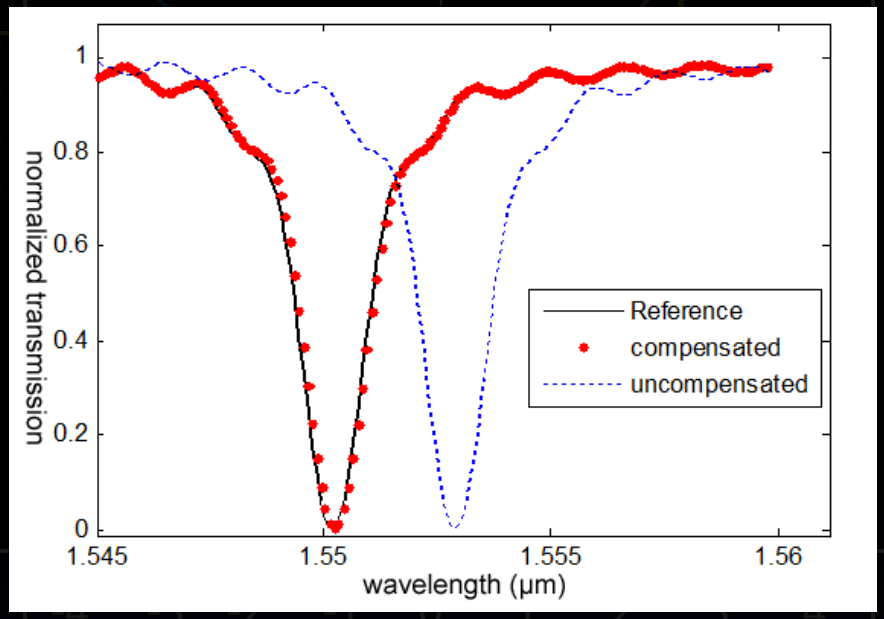
$$\beta = 2\pi n_{eff}/\lambda_0 \qquad \lambda = \lambda_0/n_{eff}$$

$$L_{comp} = 2a = \frac{q\pi}{\beta} = \frac{\lambda}{2}$$

Resonant Wavelength Shift



Temperature to Notch Width



Future Work: Tremendous Opportunity

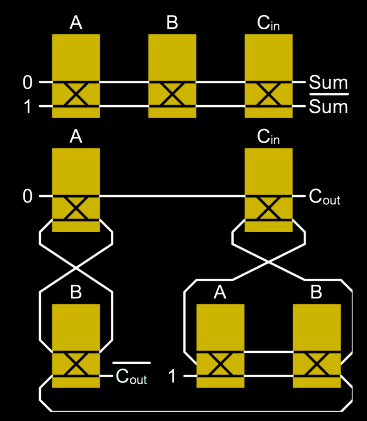
- Logic
  - Nonlinear gates, how do we use them sparingly?
  - Buffer insertion problem
- Global Routing
  - Routing Congestion in NoCs
- Abstractions of thermal gradients
  - Coordinated place-and-route, under thermal gradients
- Heat Dissipation Thermal Vias (TSVs)
  - Model as thermal-aware placement
  - Coordinate with thermal aware resynthesis for better thermal

Future Work

- Issues in Testing and Manufacturing Variability
  - Manufacturing variability changes waveguide profile
  - Will cause line-edge roughness, phase change
  - Static compensation may not be sufficient
- How to conceive failures and fault models?
- ATPG for Si-photonics?
- High sensitivity of Si photonics may require on-line test
  - Prohibitive cost may make it impossible

- ***Collaboration with D2T & VDEC: fabrication and testing of RRs with notch perturbation***

Conclusion

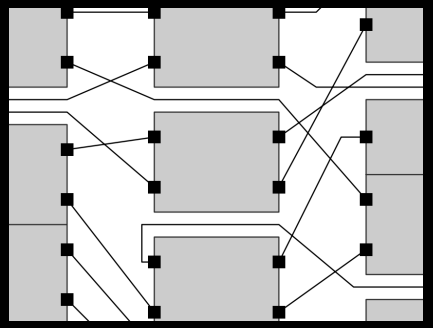


Silicon Photonics

- Greater integration
- ➢ ***Design Automation***

Logic Synthesis

- Optical logical building blocks
- ➢ Design optical networks using logic

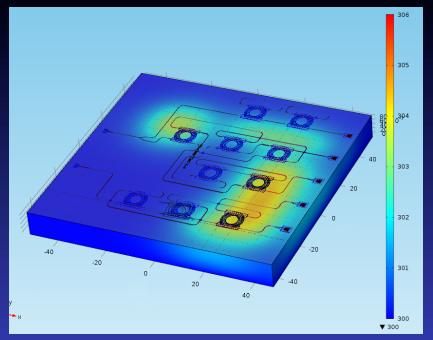


Physical Synthesis

- Hand layout to automated design
- Placement, global, channel routing
- ➢ Minimize signal loss

Thermal-aware Resynthesis

- Static compensation of sensitive devices
- Change notch width, ring length
- ➢ Reduce active tuning power



Selected Publications

- L. Schlitt, P. Kalla, S. Blair, “A Methodology for Thermal Characterization Abstraction of Integrated Opto-Electronic Layouts”, Intl. Conf. VLSI Design, India, 2016.
- C. Condrat, P. Kalla, S. Blair, “Crossing-aware Channel Routing for Integrated Optics”, IEEE TCAD, vol 33, no 5, June 2014.
- C. Condrat, P. Kalla, S. Blair, “Thermal-Aware Synthesis of Integrated Photonic Ring Resonators”, ICCAD 2014.
- C. Condrat, P. Kalla, S. Blair, “Logic Synthesis for Integrated Optics”, Great Lakes Symposium on VLSI, 2011.