ECE/CS 3700: Fundamentals of Digital System Design

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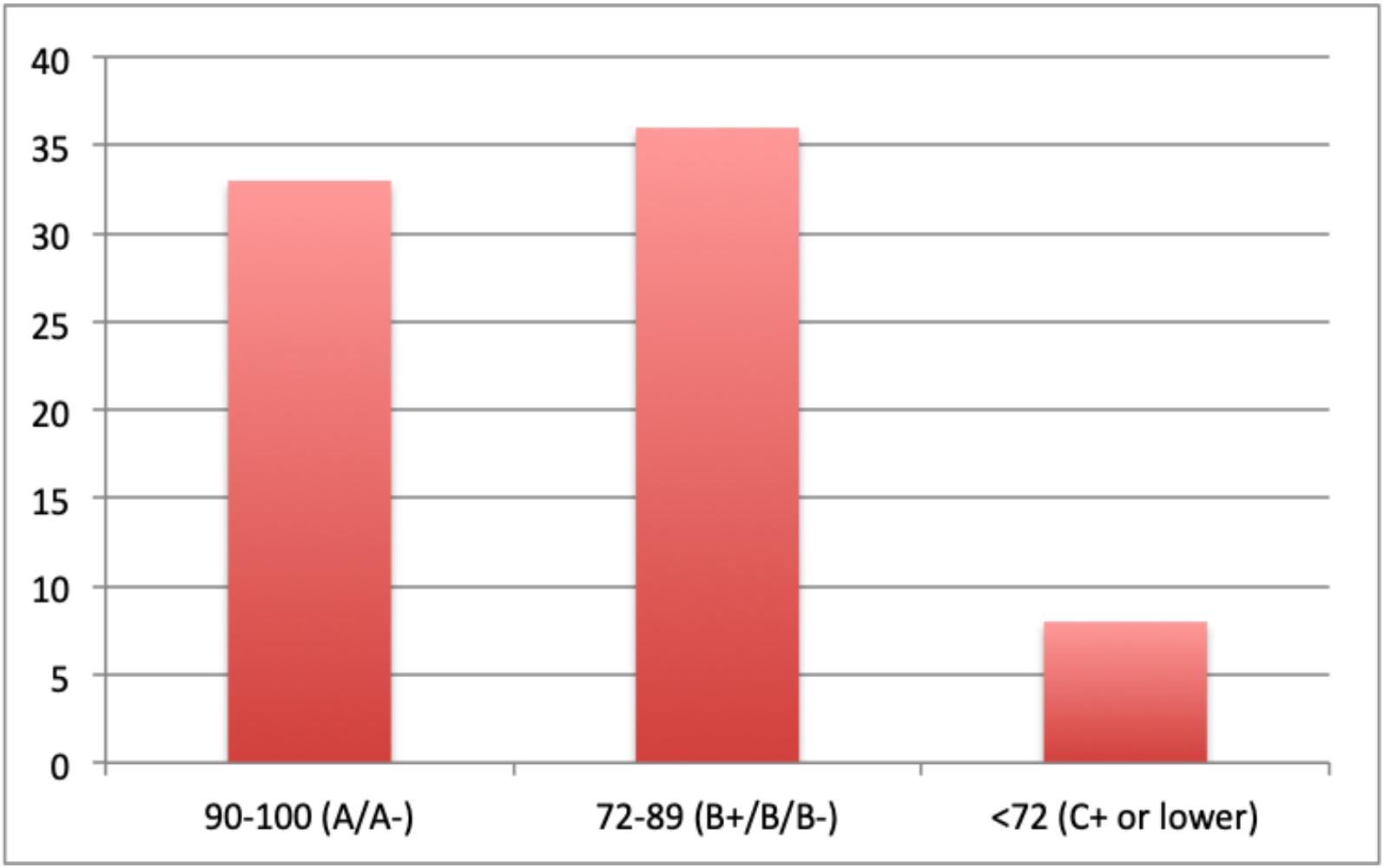
Midterm 2 Solution

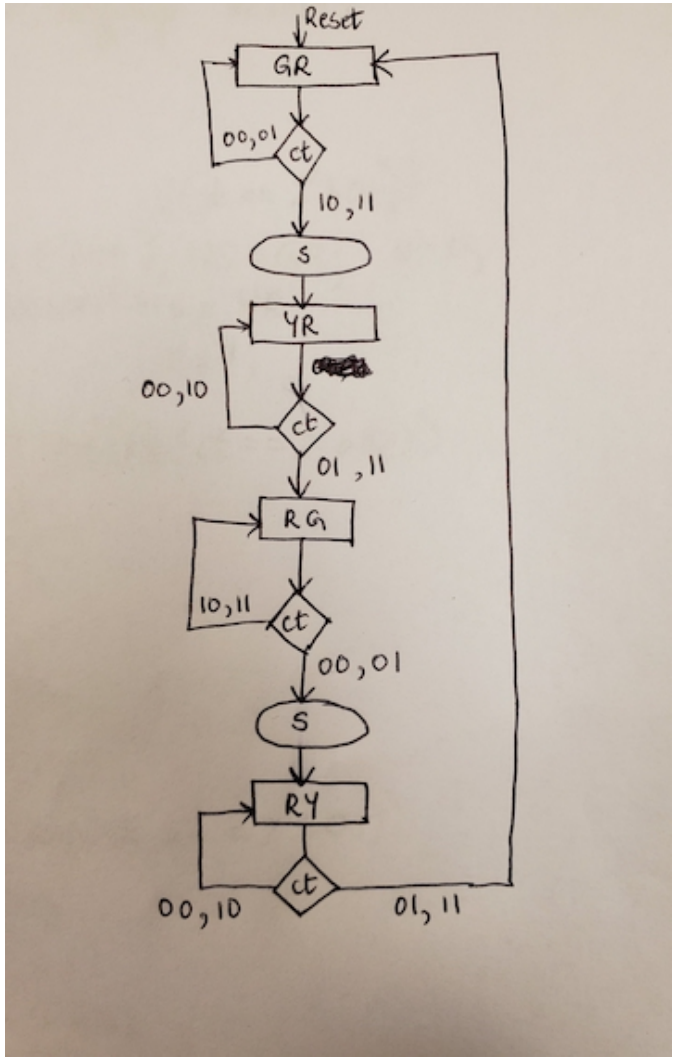
Midterm 2 Statistics



Average - 84.8

Standard deviation - 11.6

1(a) ASM Charts (Bhawna)



Perfect ASM : 15 pts, Logical flow correct, but wrong modules: 12 pts

Logical flow correct/missing output: 10 pts, Partial correct logical flow: 8 pts

1(b) Behavioral Verilog (Bhawna)

```
module FSM(input Clock, Resetn, c, t, s)
  input Clock, Resetn, c, t; // 2 points
  output s;
  reg [2,1] PS, NS;
  parameter [2:1] GR = 2'b00, YR = 2'b01, RG = 2'b10, RY = 2'b11;
  always@(posedge Clock, negedge Resetn) // 3 points
     if (Resetn) PS <= GR; else PS <= NS;
  always@(c,t,PS) // 5 pts for NS Logic, 5 pts for output
  case(PS)
  GR: if (c == 0) begin NS=GR; s = 0; end
  else begin NS=YR; s=1; end
  YR: if (t == 0) begin NS=YR; s = 0; end
  else begin NS=RG; s=0; end
  RG: if (c == 1) begin NS=RG; s = 0; end
  else begin NS=RY; s=1; end
  RY: if (t == 0) begin NS=RY; s = 0; end
  else begin NS=GR; s=0; end
  endcase
endmodule
```

1(c) Verilog Testbenches (Hari)

```
module testFSM;
  // Inputs
  reg Clock, Resetn, c,t; // 2 points
  // Outputs
  wire s; // 1 point
  // Instantiate the Unit Under Test (UUT)
  FSM uut ( .Clock(Clock), .Resetn(Resetn), .c(c), .t(t), .s(s) );
  initial begin
    Clock = 0;                  // 2 pts for initalization
    Resetn = 0; c = 0; t = 0; #12;
    Resetn = 1; #10
    c = 1; #10  // 4 pts for tests
    t = 1; #10
    t = 0; #10
    c = 0; #10
  end
  always #5 Clock = ~Clock;  // 3 points for clock
  always@(negedge Clock)  // 3 points for self-check
  // self-checking code here
```

1(d) Logic Minimization (Ke)

Present State	Next State (Y_1, Y_0)				Output s			
$y_1 y_0$	ct=00	ct=01	ct=10	ct=11	ct=00	ct=01	ct=10	ct=11
00	00	00	01	01	0	0	1	1
01	01	10	01	10	0	0	0	0
10	11	11	10	10	1	1	0	0
11	11	00	11	00	0	0	0	0

2 points for the correct state assignment table.

1(d) Logic Minimization (Ke)

Y_1 (4pts)

$y_1 y_0$ \ ct	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	0	0	1
10	1	1	1	1

Y_0 (4pts)

$y_1 y_0$ \ ct	00	01	11	10
00	0	0	1	1
01	1	0	0	1
11	1	0	0	1
10	1	1	0	0

s (4pts)

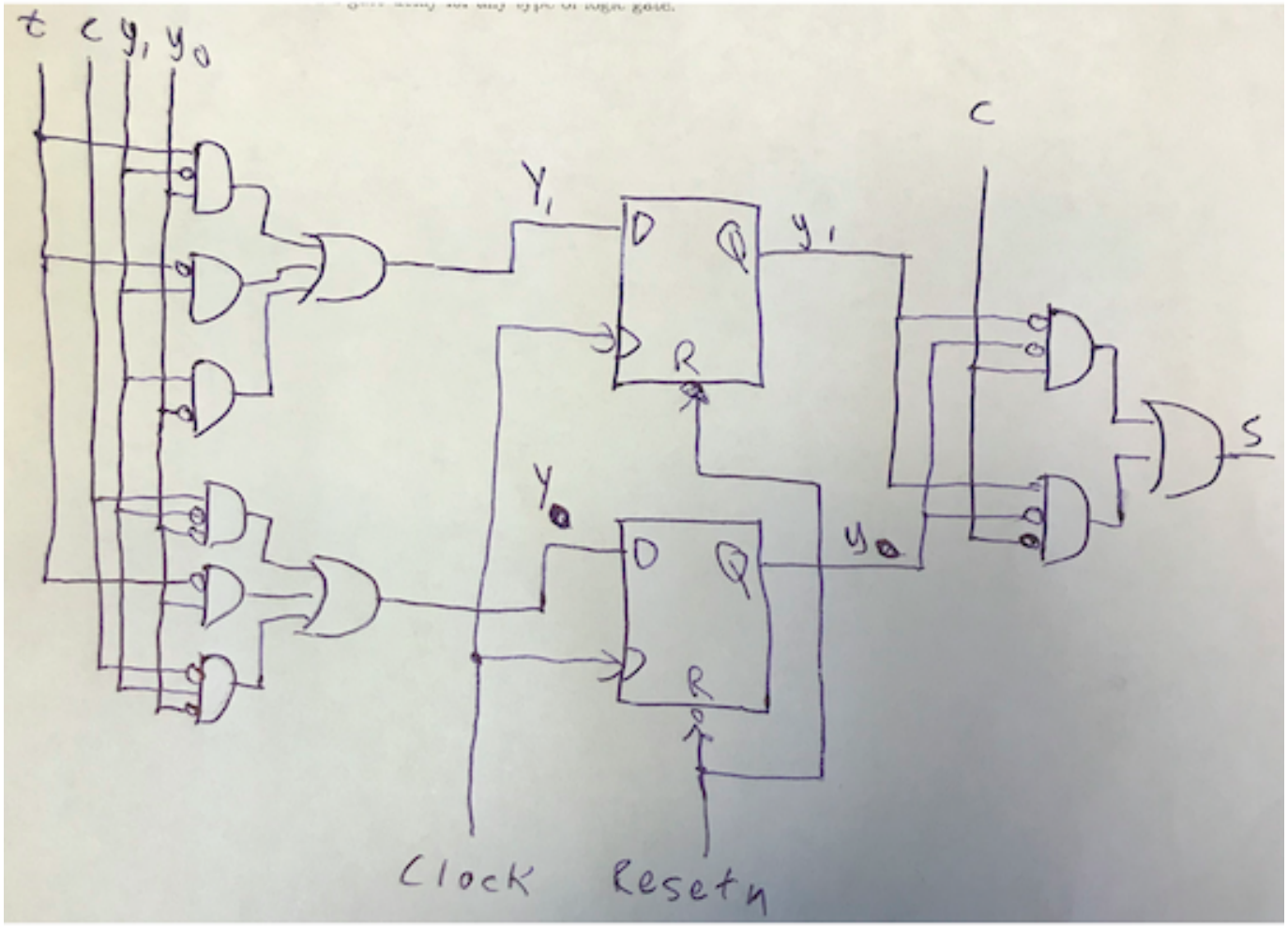
$y_1 y_0$ \ ct	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	0	0	0	0
10	1	1	0	0

$$Y_1 = t\overline{y}_1 y_0 + \overline{t} y_1 + y_1 \overline{y}_0 \text{ (2pts)}$$

$$Y_0 = c\overline{y}_1 \overline{y}_0 + \overline{t} y_0 + \overline{c} y_1 \overline{y}_0 \text{ (2pts)}$$

$$s = c\overline{y}_1 \overline{y}_0 + \overline{c} y_1 \overline{y}_0 \text{ (2pts)}$$

1(e) Timing Analysis (Chris)



$$f_{max} = 1/T_{min} = 1/(t_{path} + t_{su} + t_{cQ}) = 1/(3.2ns + 0.8ns + 1ns) \approx 200MHz$$

Schematic (10pt), Timing (5pts).

2. State Reduction (Harsha)

$$
\begin{aligned}
P_1 &= (S0, S1, S2, S3, S4, S5, S6) \quad \text{(1 point)} \\
P_2 &= (S0, S1, S2, S4, S5, S6)(S3) \quad \text{(5 points)} \\
P_3 &= (S0, S1, S2, S5, S6)(S3)(S4) \quad \text{(5 points)} \\
P_4 &= (S0, S1, S2)(S5, S6)(S3)(S4) \quad \text{(5 points)}
\end{aligned}
$$

Present State	Next state w = 0	Next state w = 1	Output z
S0	S5	S0	1
S3	S3	S0	0
S4	S3	S4	1
S5	S5	S4	1

(4 points)