# ECE/CS 3700: Fundamentals of Digital System Design

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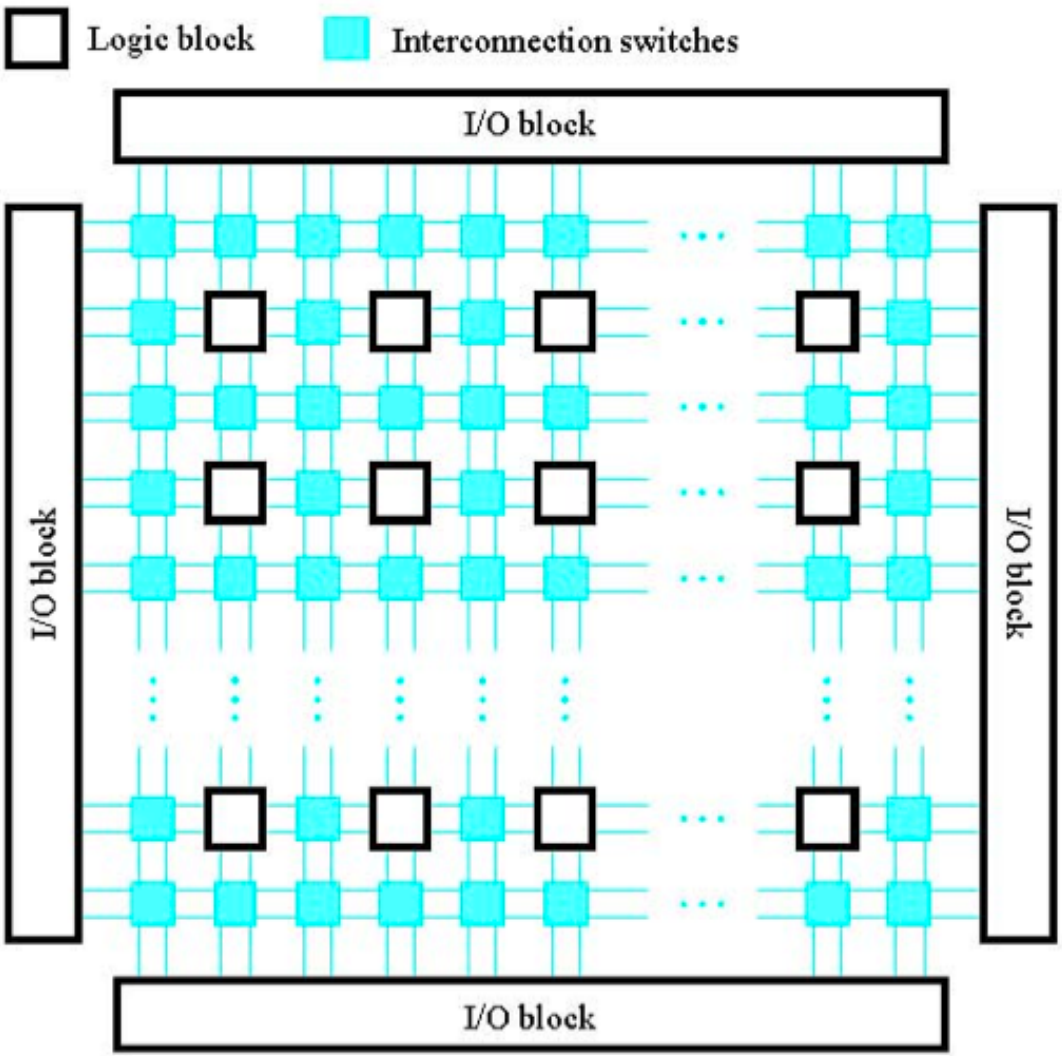
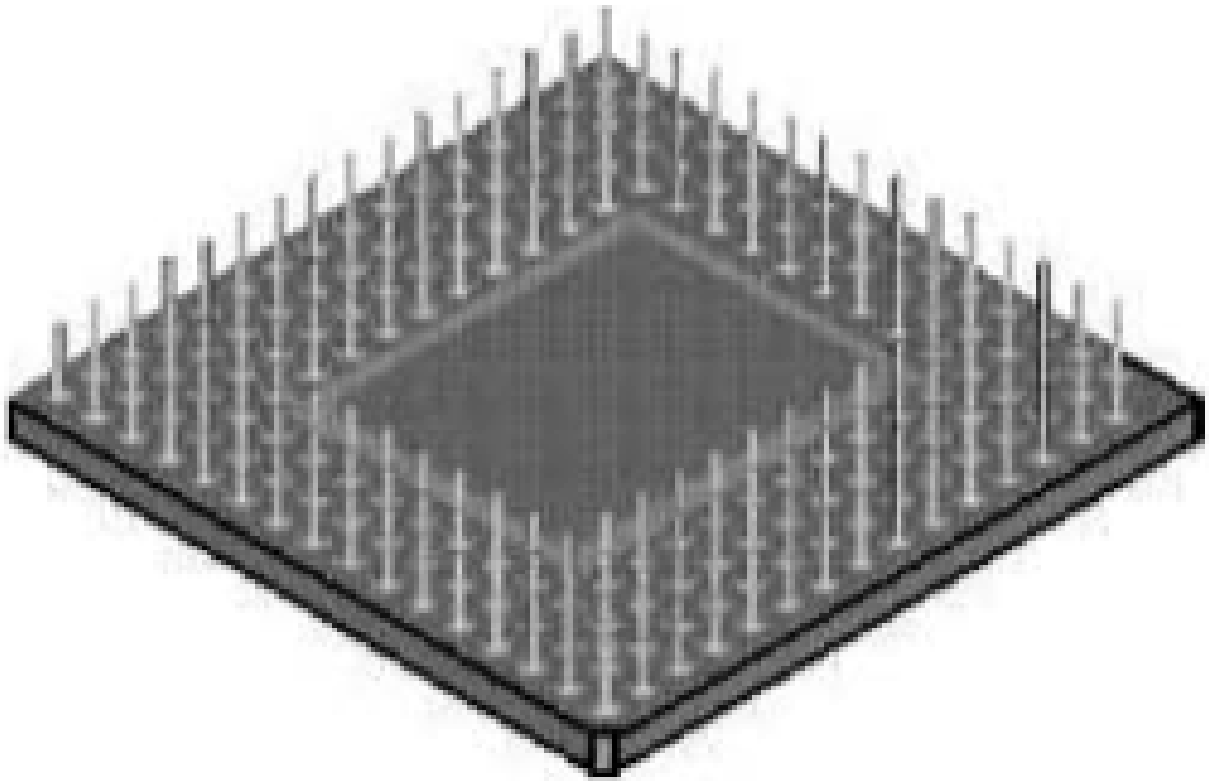
Lecture 4: Supplemental

# A Field Programmable Gate Array (FPGA)



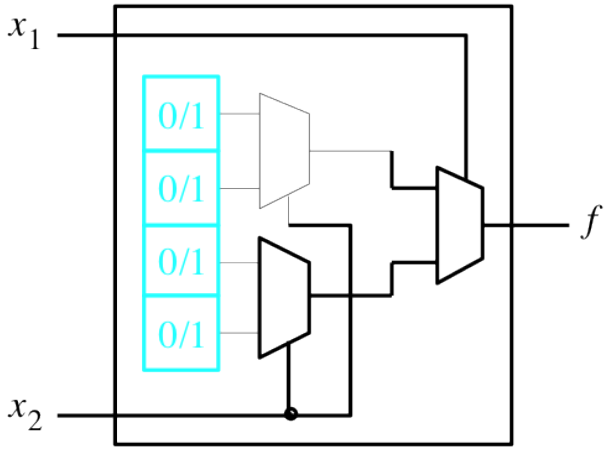

(a) General structure of an FPGA

# A Field Programmable Gate Array (FPGA)



(b) Pin grid array (PGA) package (bottom view)

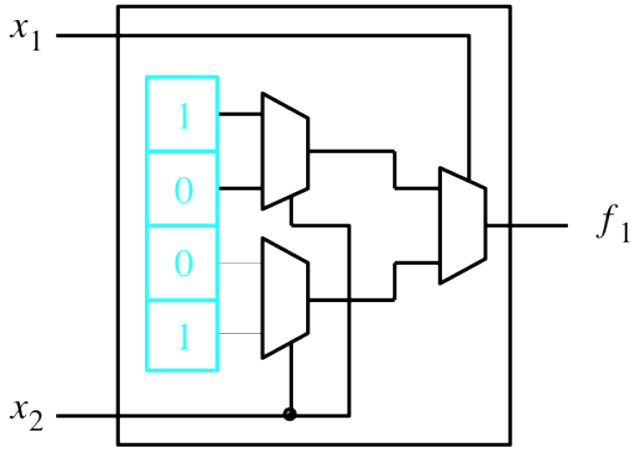
# A Two-input Lookup Table (LUT)




(a) Circuit for a two-input LUT

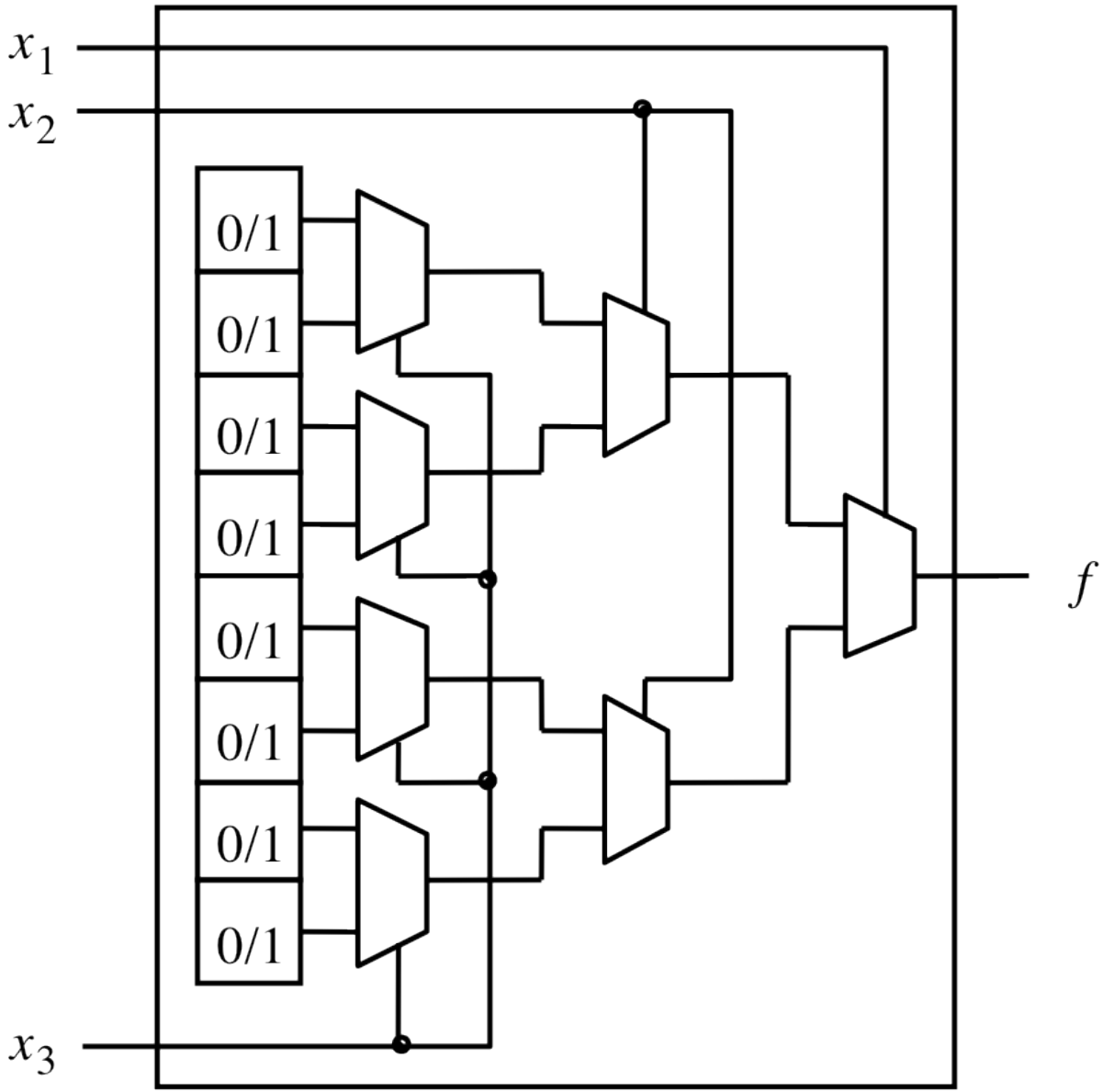
| $x_1$ | $x_2$ | $f_1$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$

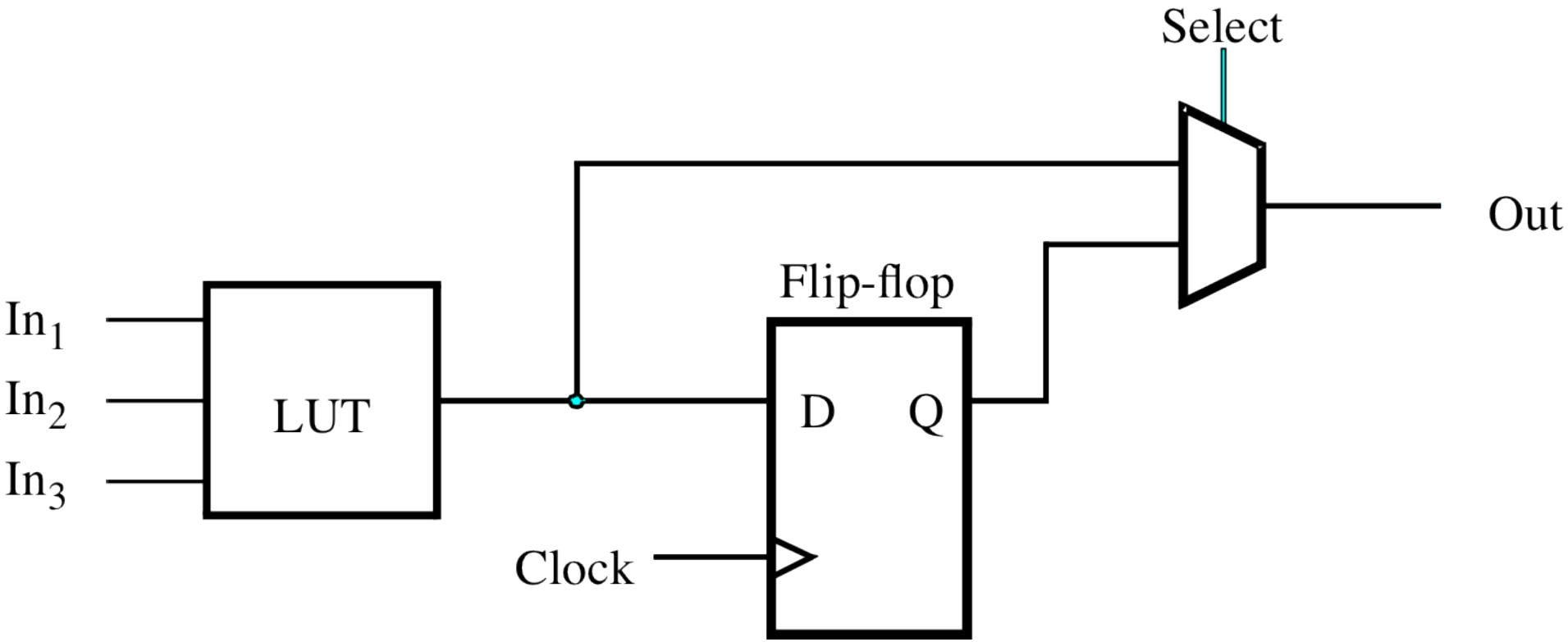



(c) Storage cell contents in the LUT

# A Three-input LUT

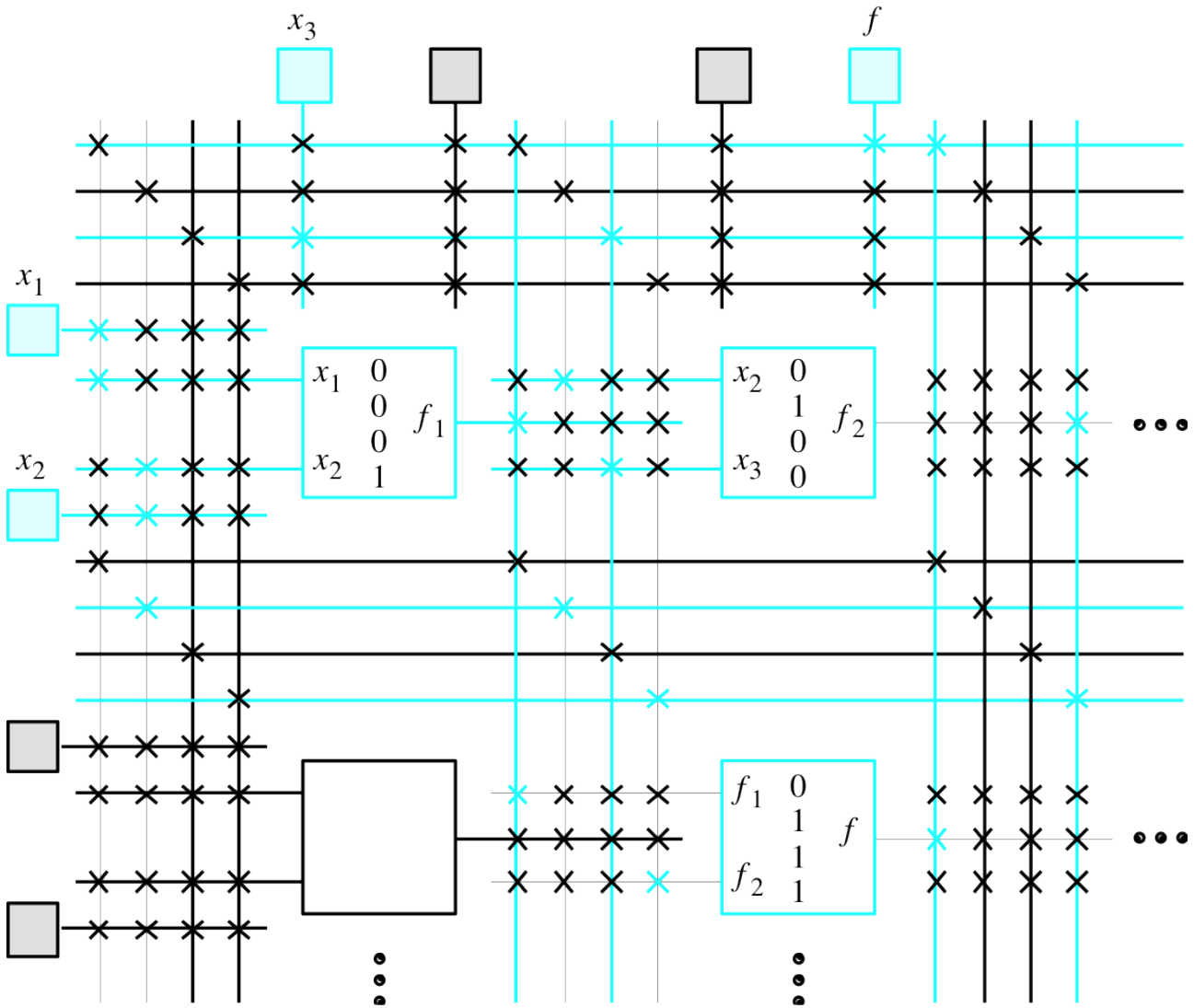


# A Flip-flop in an FPGA Logic Block

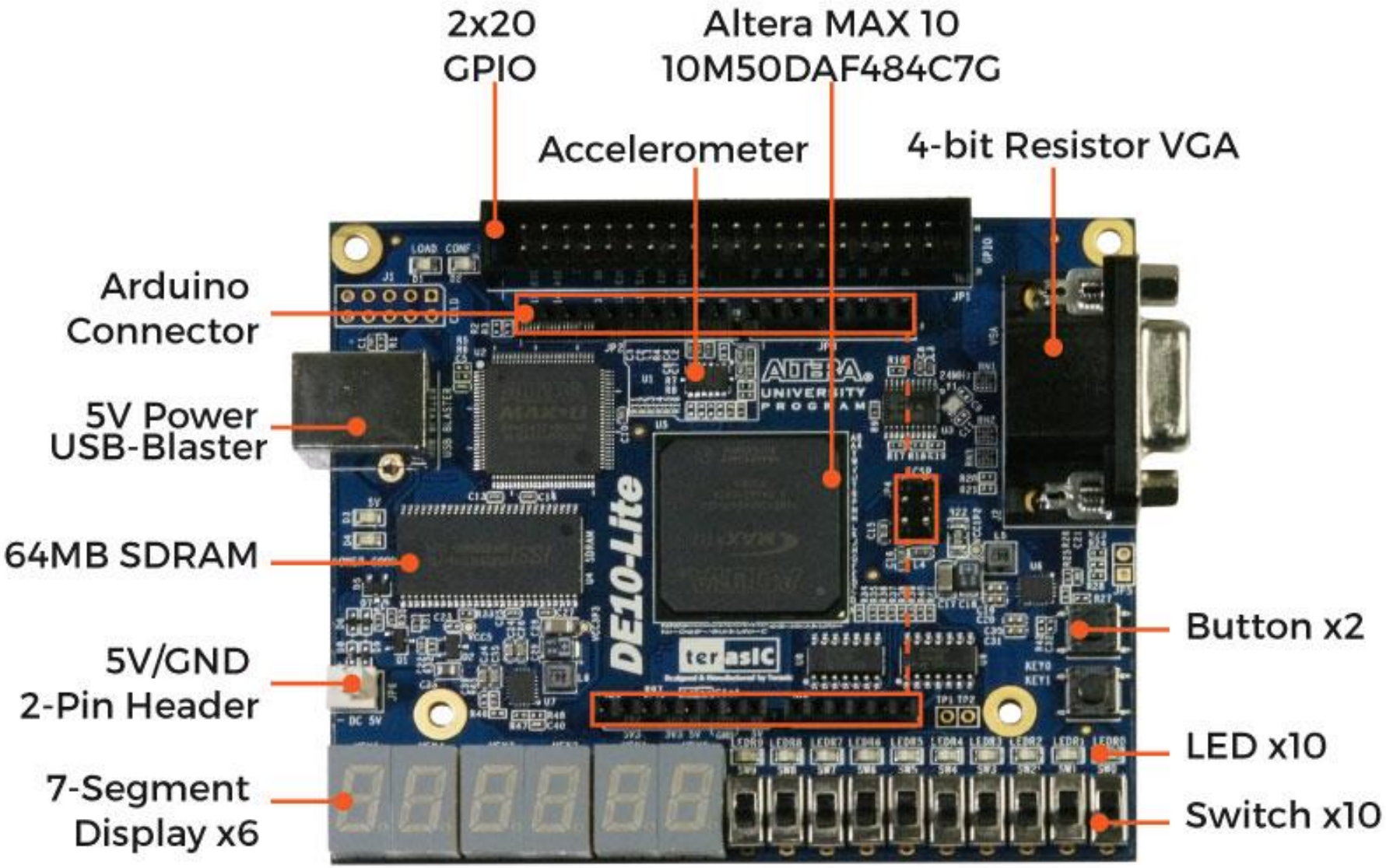


# A Section of a Programmed FPGA

$$f_1 = x_1 x_2 \quad f_2 = \overline{x}_2 x_3 \quad f = f_1 + f_2$$



# DE10-Lite Board



# DE10-Lite FPGA

- Altera MAX 10 10M50DAF484C7G Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1,638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18 $\times$ 18 Multiplier
- 4 PLLs

# Logical Elements (LEs)

## Intel MAX 10 Device Family LEs