

Engineering Genetic Circuits

Chris J. Myers

Lecture 12: Genetic Circuit Technology Mapping

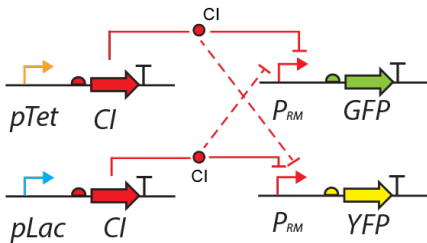
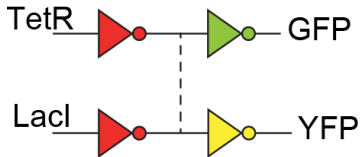
Genetic Circuit Designs

- Genetic circuits are created from biological components that mimic the behavior of Boolean logic gates.
- Genetic circuits can be built inside of a living organism (*in vivo*) or in a test tube (*in vitro*).
- Most genetic circuits that have been built are **combinational circuits**: input signals map to output signal.
- Outside of combinational circuits, memory circuits that have been constructed for **sequential circuits**: input signals are combined with states to produce the output signal.

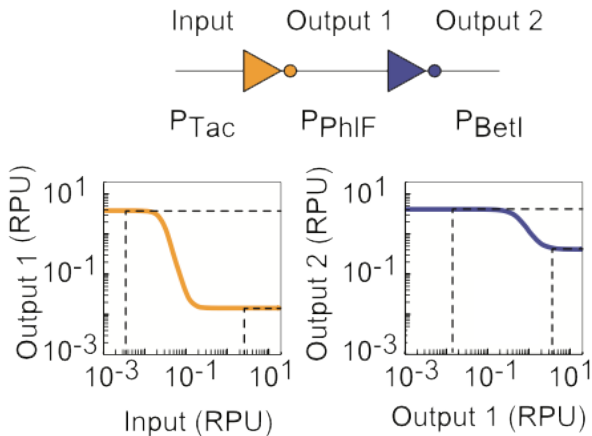
Genetic Constraints

- Crosstalk
- Signal Mismatch
- Roadblocking
- Genetic Context Effects

Crosstalk

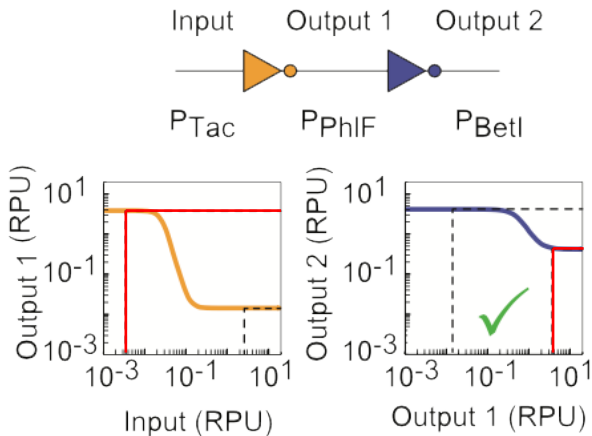


Signal Mismatch



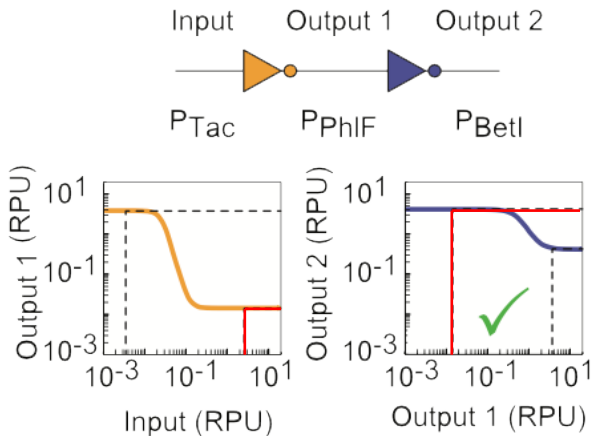
Nielsen et al., *Science*, 2016

Signal Mismatch



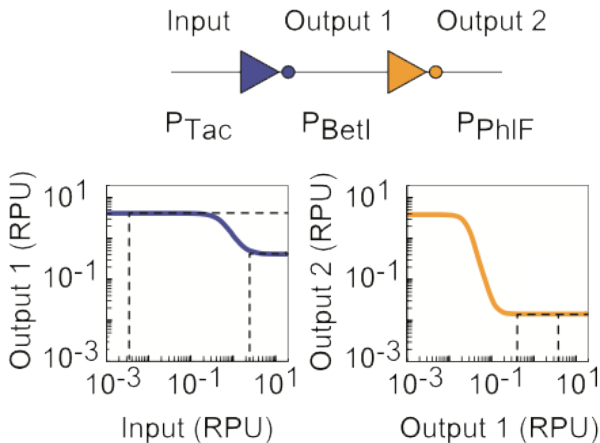
Nielsen et al., *Science*, 2016

Signal Mismatch



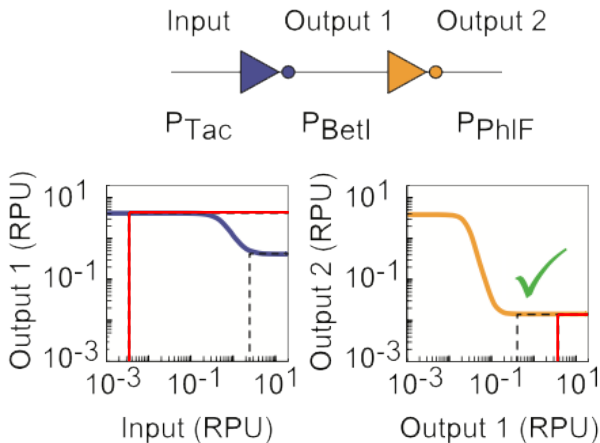
Nielsen et al., *Science*, 2016

Signal Mismatch



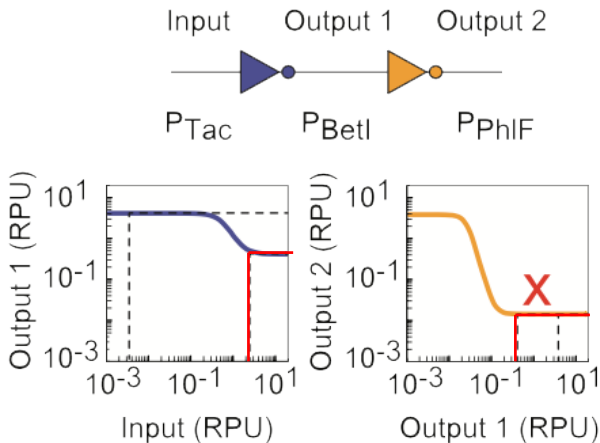
Nielsen et al., *Science*, 2016

Signal Mismatch



Nielsen et al., *Science*, 2016

Signal Mismatch



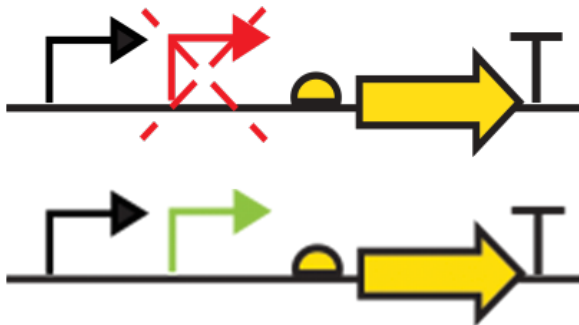
Nielsen et al., *Science*, 2016

Roadblocking



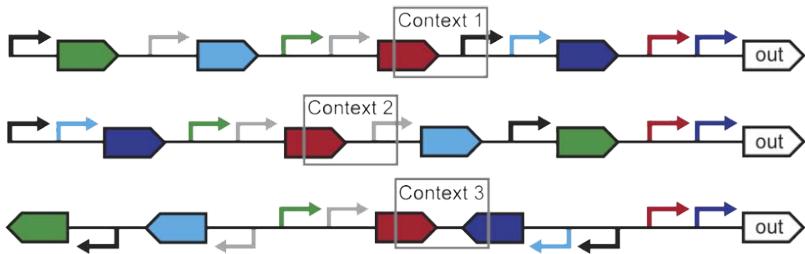
Nielsen et al., *Science*, 2016

Roadblocking



Nielsen et al., *Science*, 2016

Genetic Context Effects



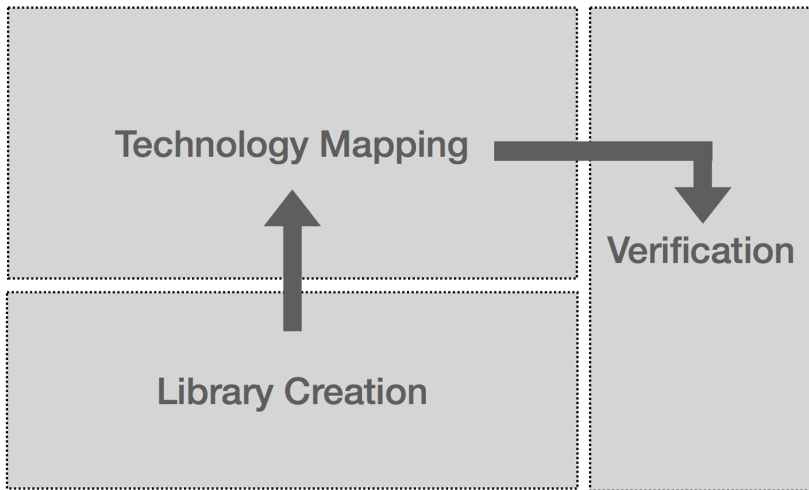
Vaidyanathan et al., *IEEE*, 2015

Automation and Computer Aided Design (CAD) tools

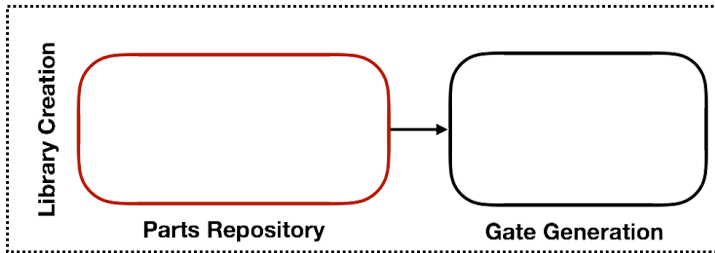
- Logic gates are used to build complex circuits.
- Complex circuit is described in some form of specification.
- Building complex circuit that meets the specification is time consuming.
- Design automation will help refine the design space before building a productive circuit to meet the specification (description of the circuit) goal.
- Models can be generated programatically through CAD tools.
- Analysis of models can help evaluate design alternatives on a computer (*in silico*).

- Technology mapping process assigns physical biological parts to implement the functional design specification.
- Existing technology mapping frameworks have accounted for genetic design constraints.

Technology Mapping Template



Library Creation



- Biological parts are encoded into data standards and have been deposited onto online repositories for programmable access.

Data Standards

combine the computational modeling in biology network

Knowledge

Model

Visualization

Core Data Standards

SBOL

BioPAX

SED ML

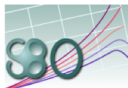
SOML

CellML

SBOL VISUAL

SOGN

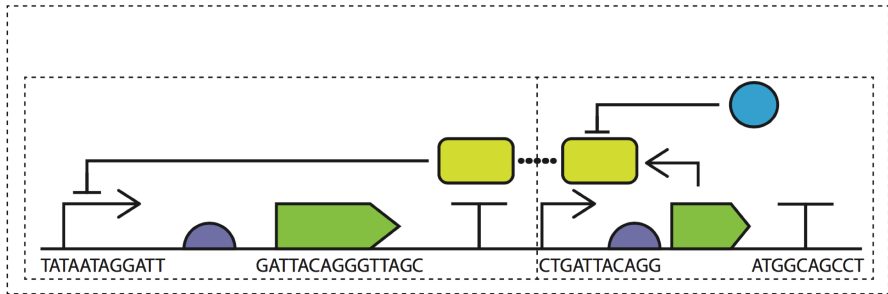
Associated Standardization Efforts



BioModels.net
Qualifiers

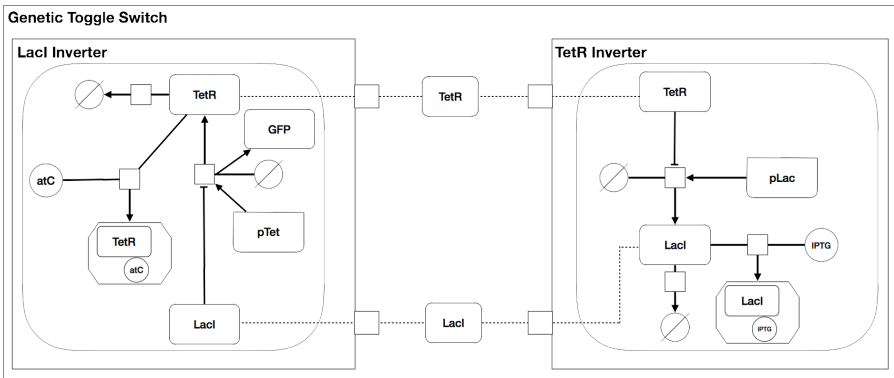
Synthetic Biology Open Language (SBOL)

- An **open standard** for representing *in silico* **biological designs**.

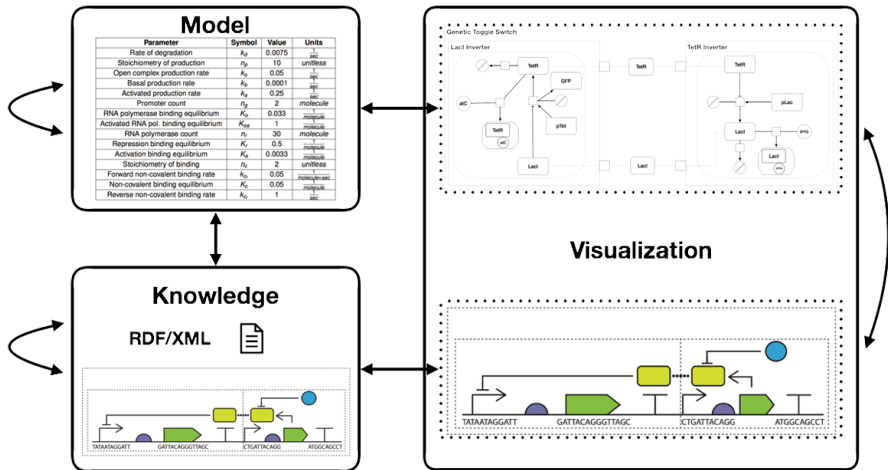


Systems Biology Markup Language (SBML)

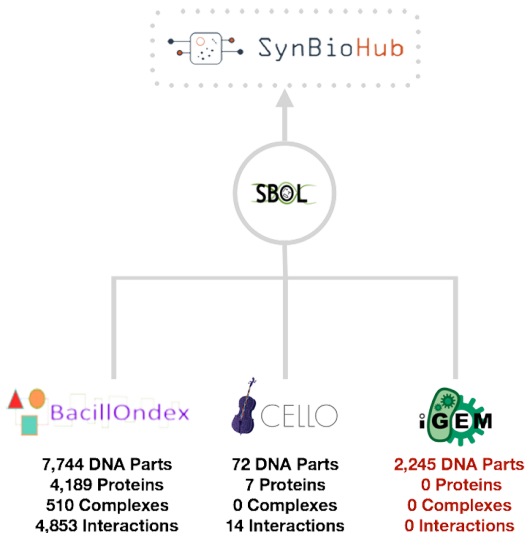
- An **open standard** to describe the behavioral models of **biological systems**.



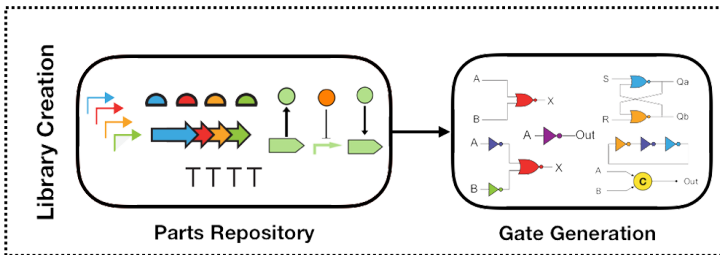
Data Standard Conversions



Available Datasets

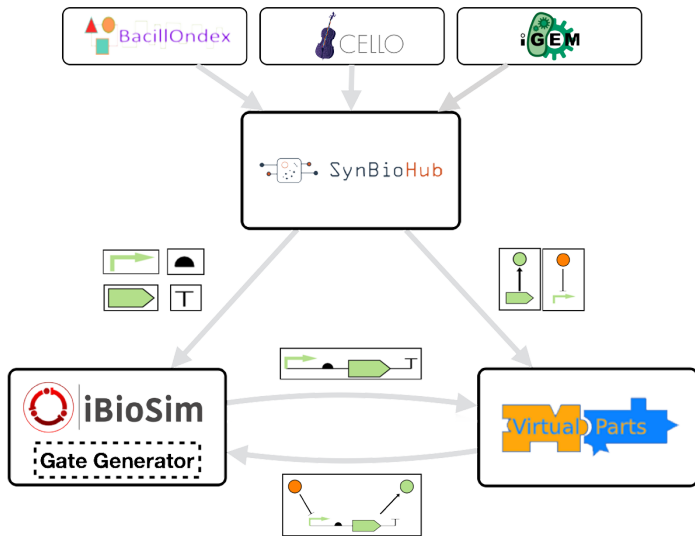


Gate Generation

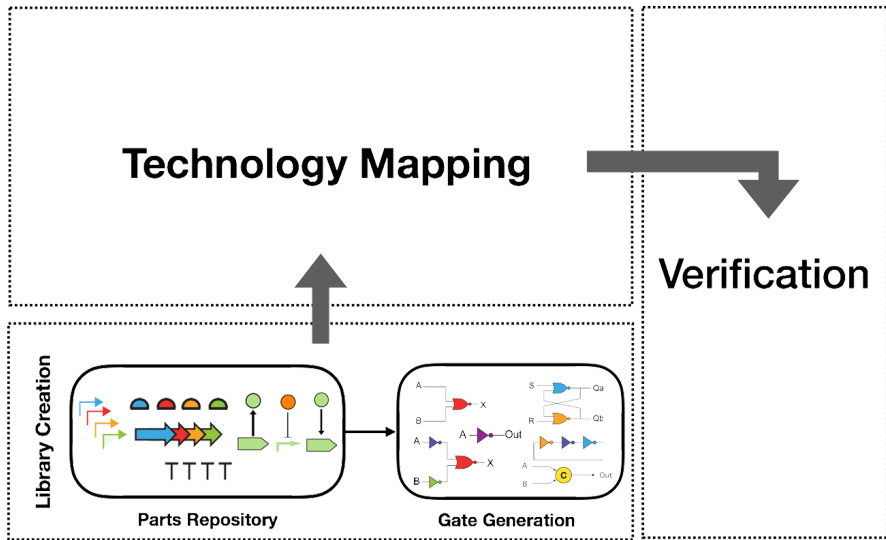


- Gate generation automates the process of producing gates from a library of parts.

Automating Library Creation



Library Creation



Existing Technology Mapping

	MatchMaker ¹	SBROME ²	iBioSim ³	Cello ⁴	GeneTech ⁵
Specification Type	Abstract genetic regulatory network	Abstract genetic regulatory network	Abstract genetic regulatory network	Verilog	Boolean expressions
Support COMBINE Standard	SBOL1	–	SBOL2 and SBML	SBOL2	–
Library	Arbitrary logic gates	Parts	Arbitrary logic gates	NOT and NOR gates	NOT and NOR gates
Signal Mismatch	✓	✗	✗	✓	✗
Crosstalk	✗	✓	✓	✓	✓
Genetic Context Effects	✗	✗	✗	✓	✗
Roadblock	✗	✗	✗	✓	✗

✓ Supported in tool.

✗ Not supported in tool.

¹ Yaman et al, *ACS Publications*, 2012

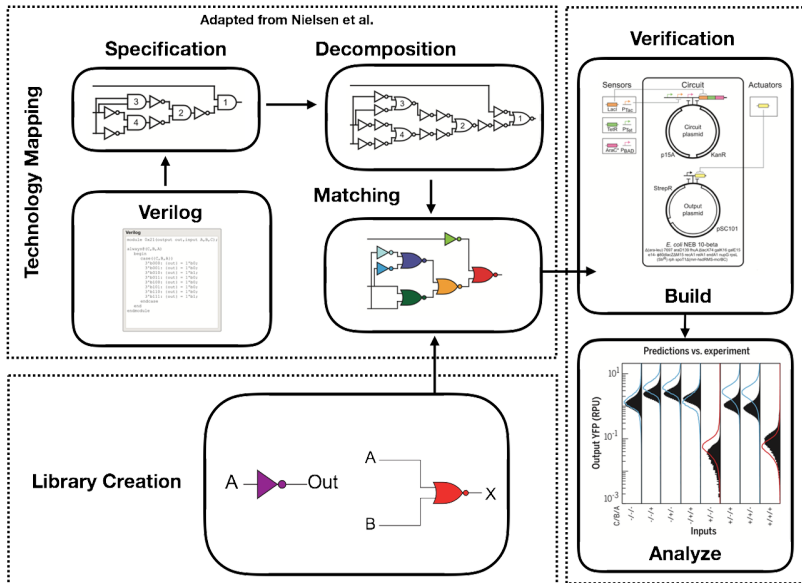
² Huynh et al., *ACS Synthetic Biology*, 2013

³ Roehner et al., *ACS Synthetic Biology*, 2014

⁴ Nielsen et al., *Science*, 2016

⁵ Baig et al., *9th International Workshop on Bio-Design Automation*, 2017

Cello's Technology Mapping



Overview of Cello

A

Cello design specification

Sensors

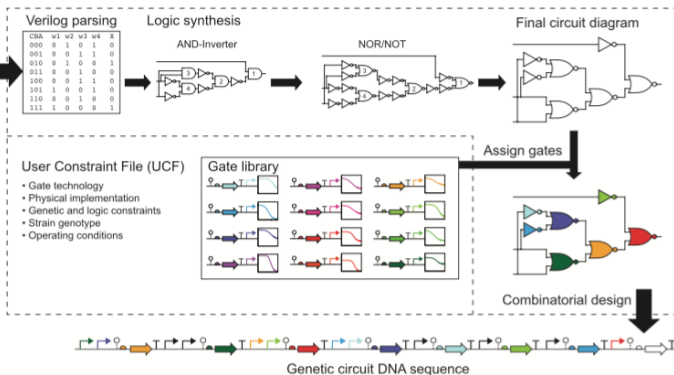
name	low	high	promoter sequence
PTac	0.003	2.8	AACGATGTTTGGCTGTTTGGAGTAAATGACG
PTet	0.001	4.4	TACTCCGCGCTTTGGCTTTTCCCTATCGAGTA
PEAD	0.008	2.5	TCTTTTCTACTCTCCGCGCTTCGAGGAGAACT

Verilog

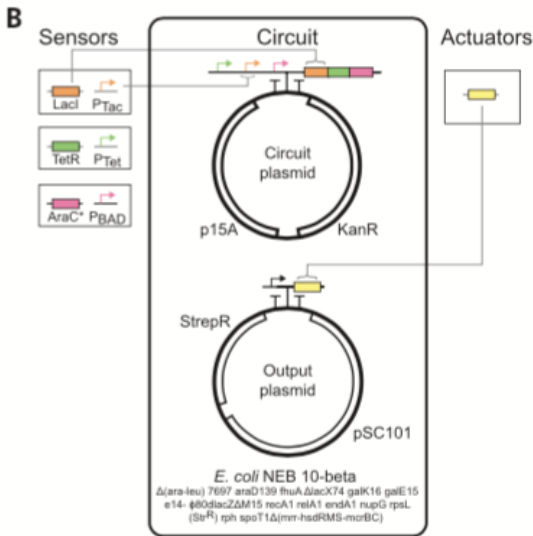
```

module 0x21(output out,input A,B,C);
begin
  case((C,B,A))
    3'b000: (out) = 1'b0;
    3'b001: (out) = 1'b0;
    3'b010: (out) = 1'b1;
    3'b011: (out) = 1'b0;
    3'b100: (out) = 1'b0;
    3'b101: (out) = 1'b0;
    3'b110: (out) = 1'b0;
    3'b111: (out) = 1'b1;
  endcase
end
endmodule
        
```

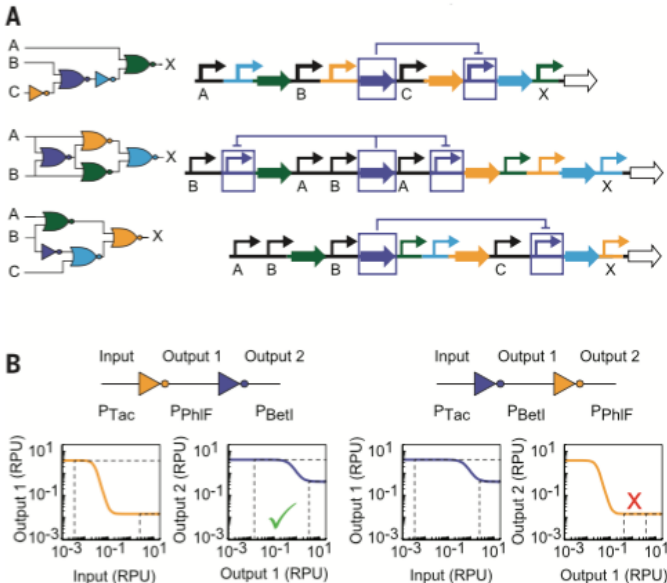
Run



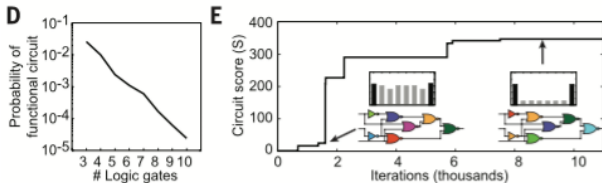
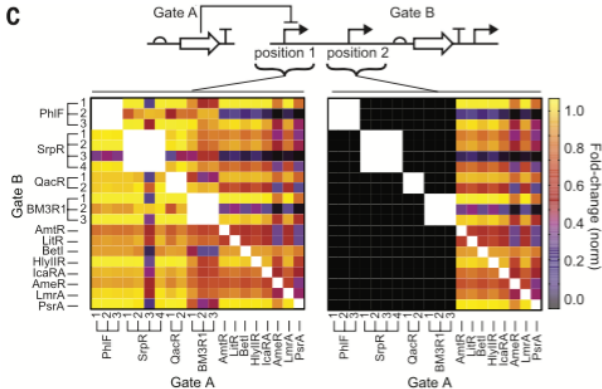
Overview of Cello (cont)



Genetic Gate Assignment



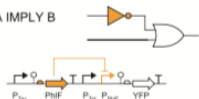
Genetic Gate Assignment (cont)



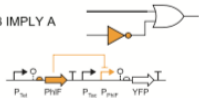
Impact of Gate Isolation

A

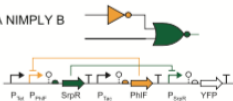
A IMPLY B



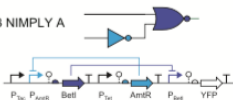
B IMPLY A



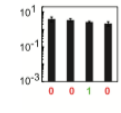
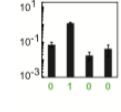
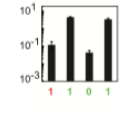
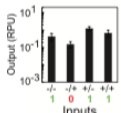
A NIMPLY B



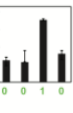
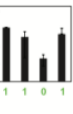
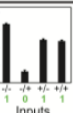
B NIMPLY A



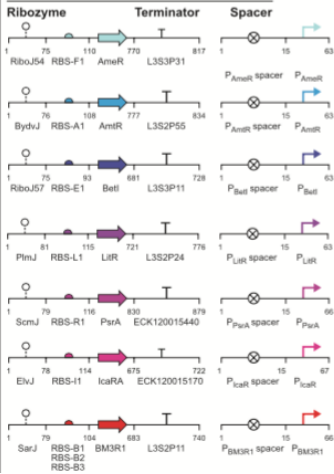
Non-insulated



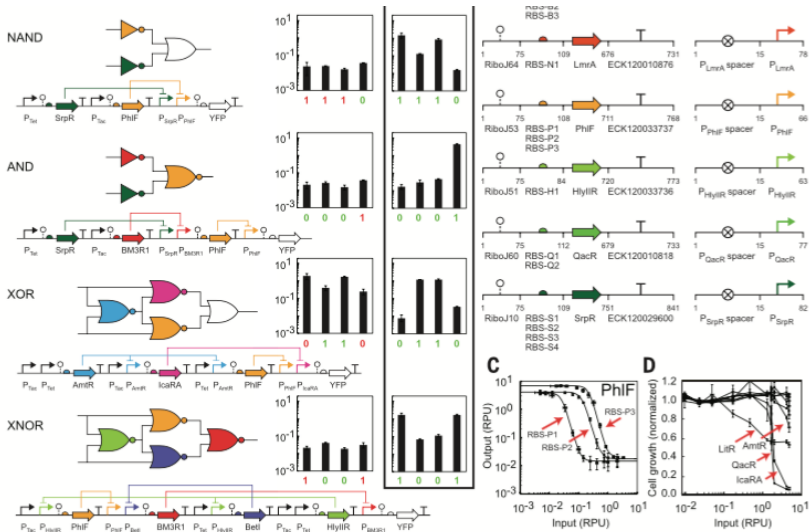
Insulated



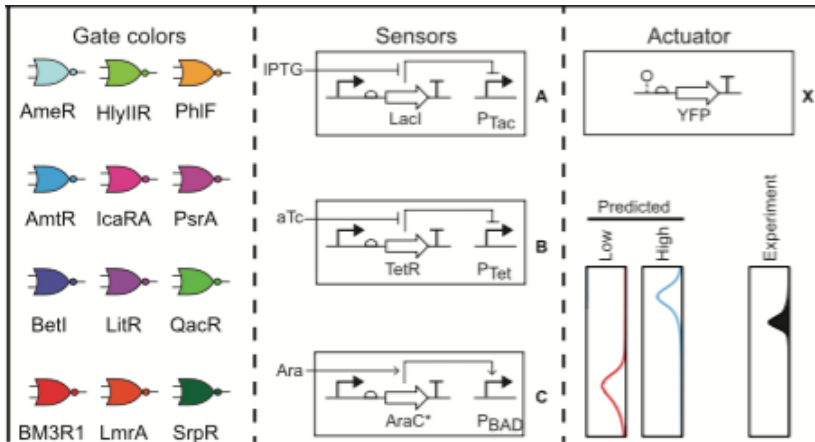
B Insulators



Impact of Gate Isolation (cont)



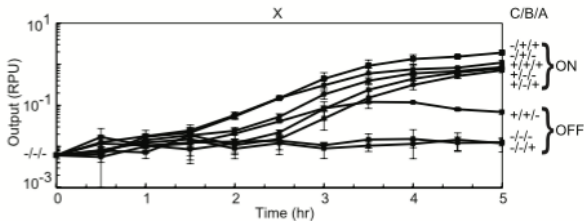
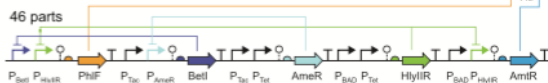
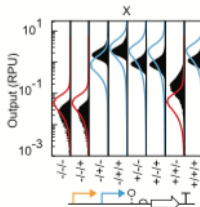
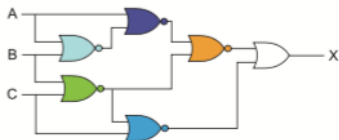
Cello Gate Library



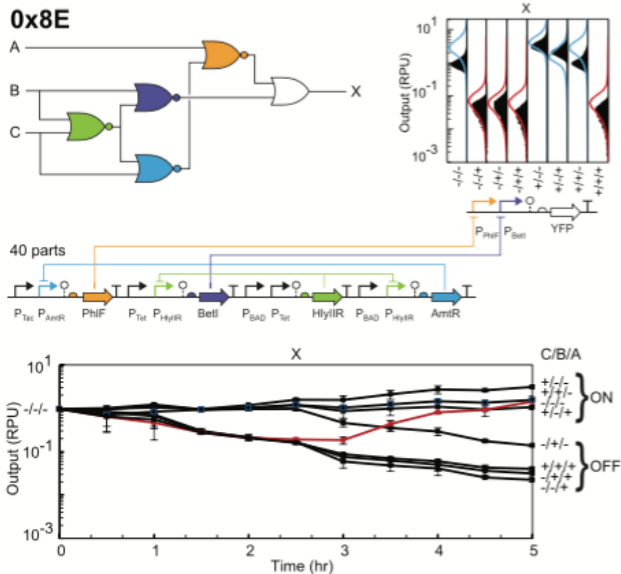
Cello Circuit Example 1

B

0x3D



Cello Circuit Example 2



Cello Priority Detector

A

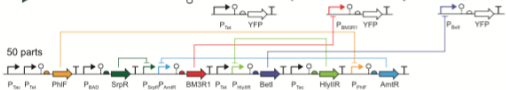
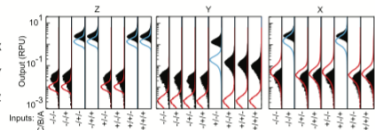
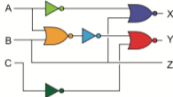
Priority detector

```

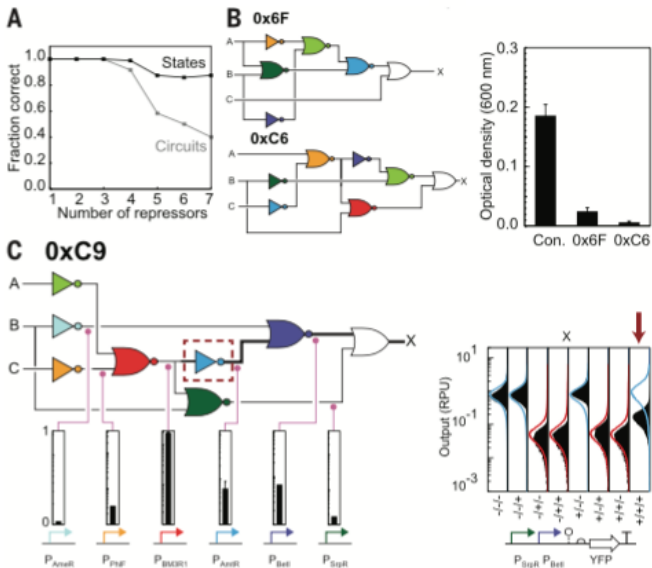
module priority_detector(output outZ, outY, outX, input
C, R, A);
always @(C,R,A)
begin
    case ({C,R,A})
        3'b000: (outZ,outY,outX) = 3'b000;
        3'b001: (outZ,outY,outX) = 3'b001;
        3'b010: (outZ,outY,outX) = 3'b100;
        3'b011: (outZ,outY,outX) = 3'b100;
        3'b100: (outZ,outY,outX) = 3'b010;
        3'b101: (outZ,outY,outX) = 3'b001;
        3'b110: (outZ,outY,outX) = 3'b100;
        3'b111: (outZ,outY,outX) = 3'b100;
    endcase
end
endmodule

```

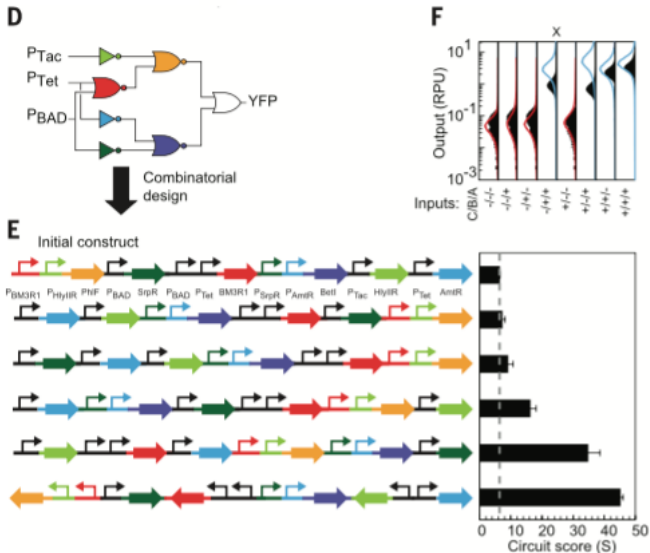
input	low	high
A.IPTG	0.003	2.8
B.aTc	0.001	4.4
C.Ara	0.008	2.5



Analysis of Circuit Failures



Analysis of Circuit Failures (cont)



Cello
Verilog
Options
Results
About
You are logged in as **myers**
Logout

Verilog
choose

```

1 module A(output out1, input in1, in2);
2   always@(in1,in2)
3   begin
4     case({in1,in2})
5       2'b00: {out1} = 1'b0;
6       2'b01: {out1} = 1'b0;
7       2'b10: {out1} = 1'b0;
8       2'b11: {out1} = 1'b1;
9     endcase
10  end
11 endmodule
12

```

design name

Run

Inputs

choose
clear

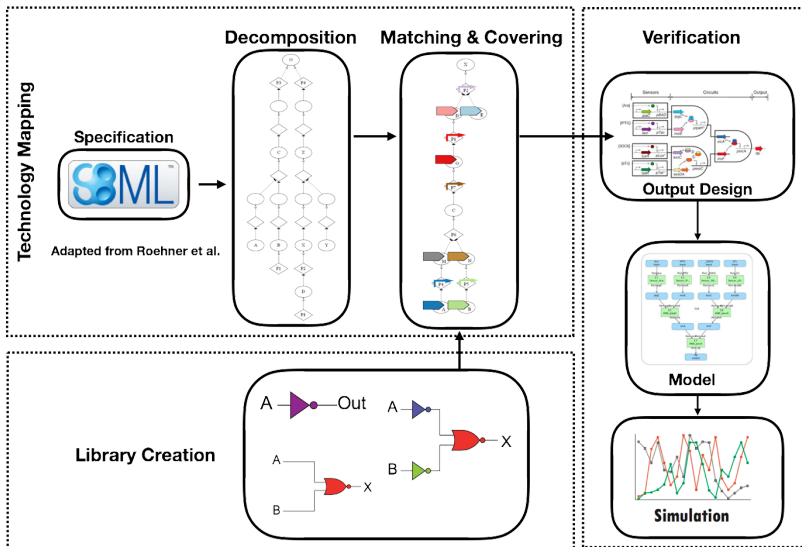
index	name	low RPU	high RPU	DNA sequence
1	pTac	0.0034	2.8	AACGATCGTTGGCTGTGTTGACA
2	pTet	0.0013	4.4	TACTCCACCGTTGGCTTTTTTCCC

Outputs

choose
clear

index	name	DNA sequence
1	YFP	CTGAAGCTGTCACCGGATGTGCTTCCGGTCTGATGAGTCCG

iBioSim's Technology Mapping



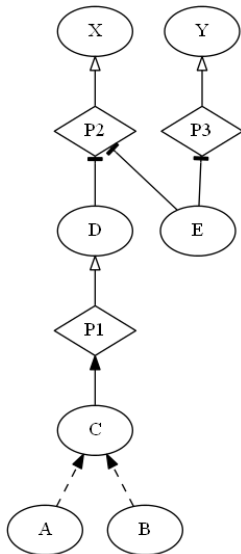
DAG-Based Technology Mapping

- 1 DAG Representation
- 2 Partitioning and Decomposition
- 3 Matching and Covering

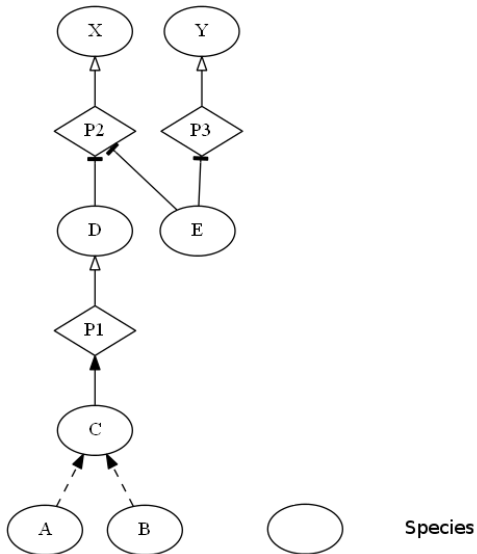
DAG-Based Technology Mapping

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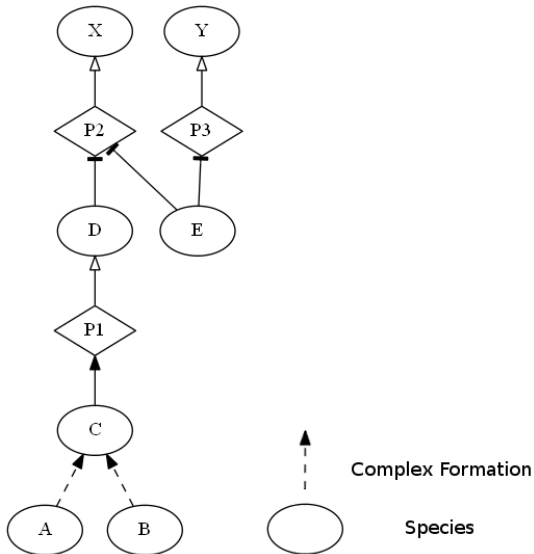
DAG Representation of Specification



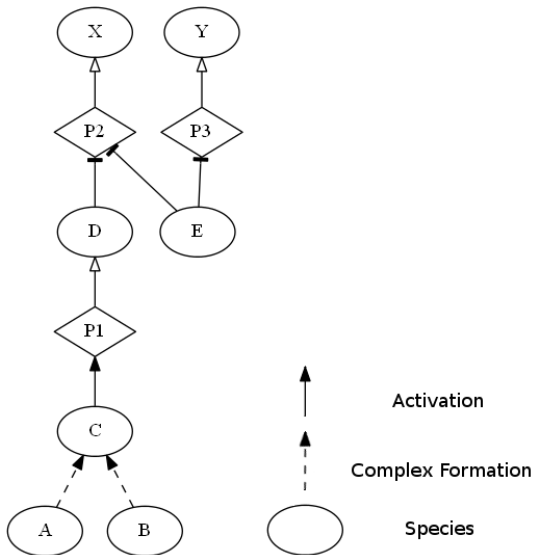
DAG Representation of Specification



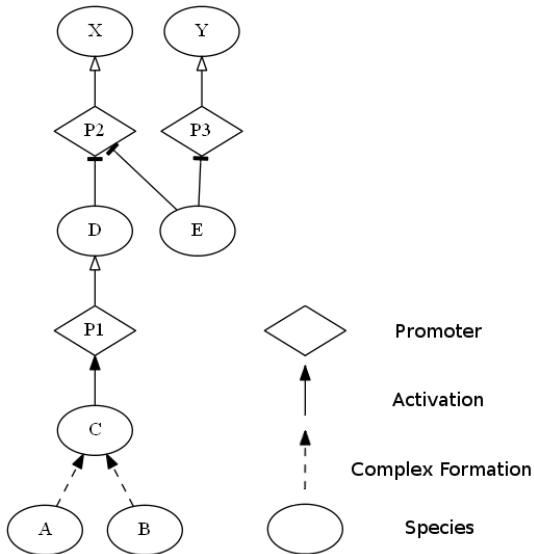
DAG Representation of Specification



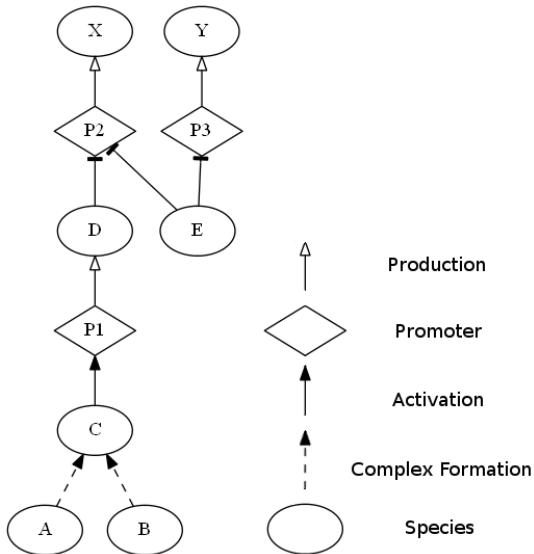
DAG Representation of Specification



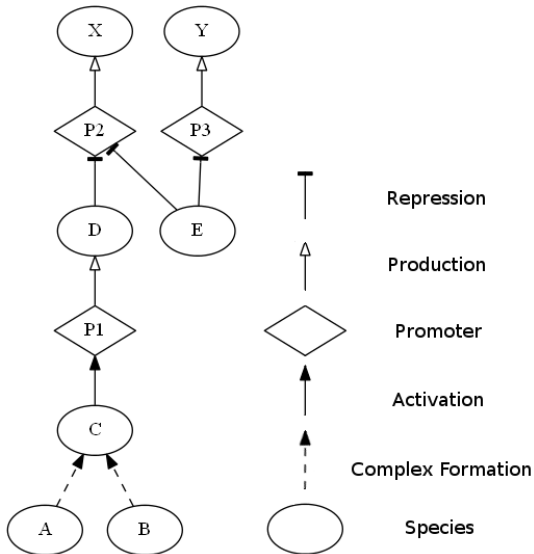
DAG Representation of Specification

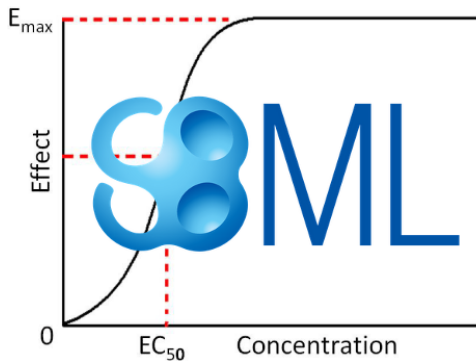


DAG Representation of Specification

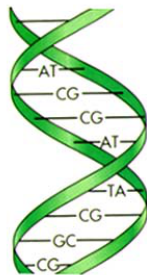


DAG Representation of Specification

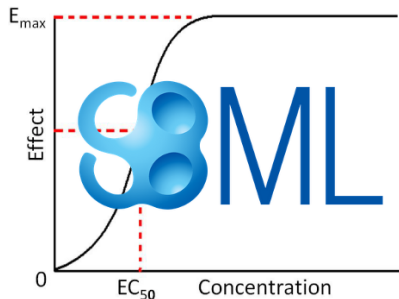




RDF/XML
Annotation



Roehner et al., ACS Synthetic Biology (2013).

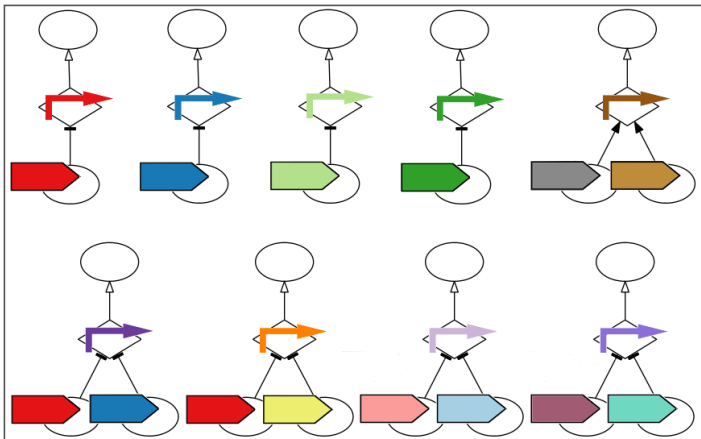


RDF/XML
Annotation



Roehner et al., ACS Synthetic Biology (2013).

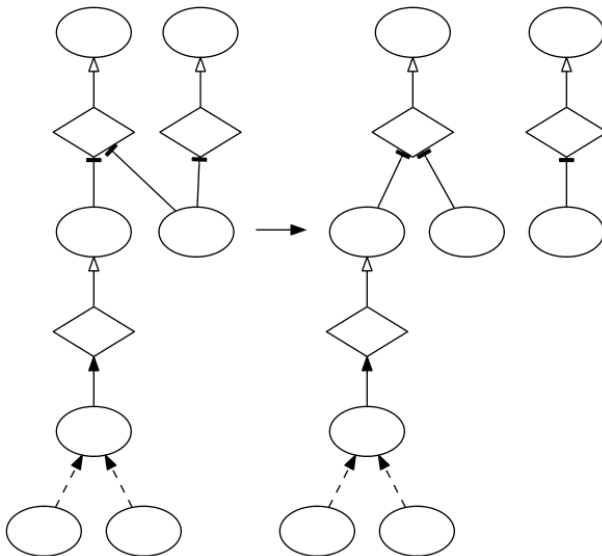
DAG Representation of Library



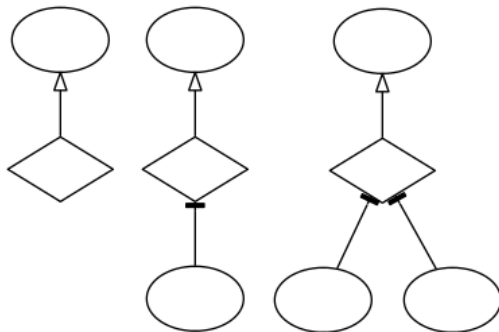
DAG-Based Technology Mapping

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- 3 Matching and Covering

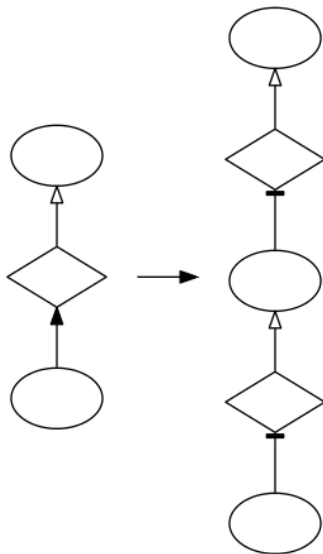
Partitioning of Specification



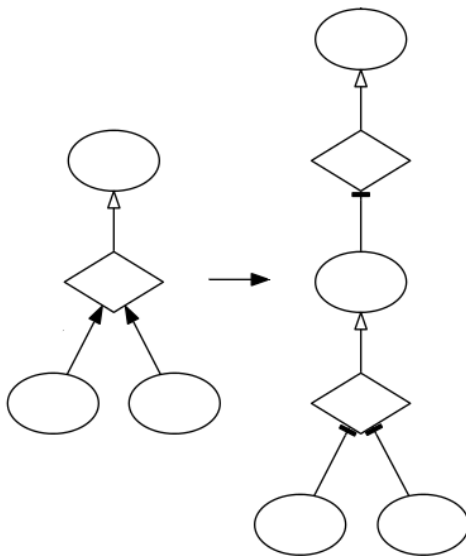
Decomposition into Canonical Form



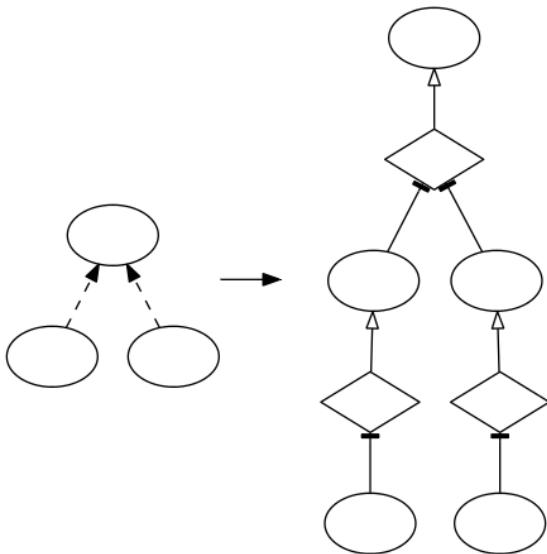
Decomposition of Activation



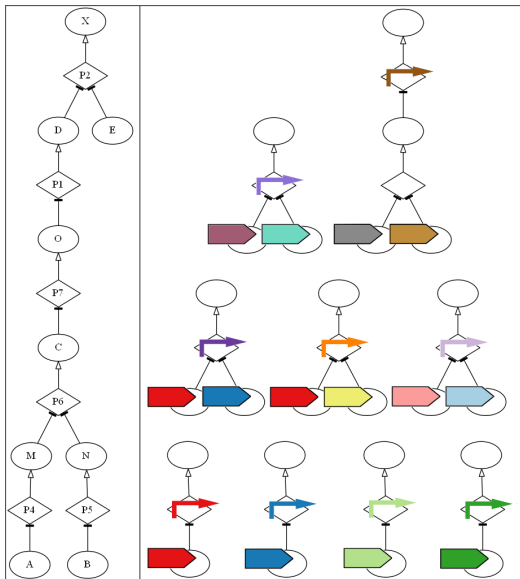
Decomposition of Dual Activation (OR Gate)



Decomposition of Complex Formation (AND Gate)



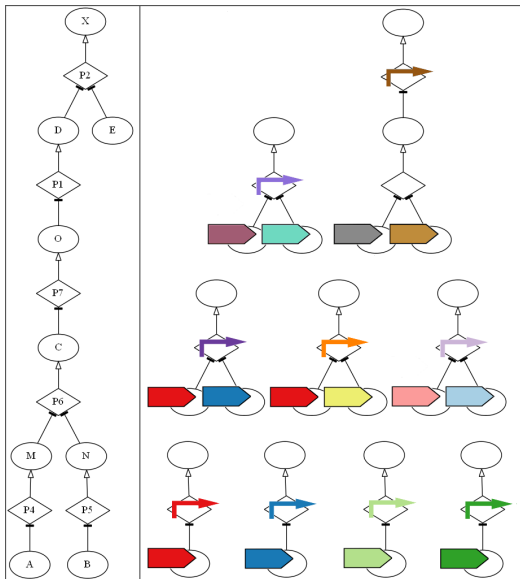
Partitioned, Decomposed Specification and Library



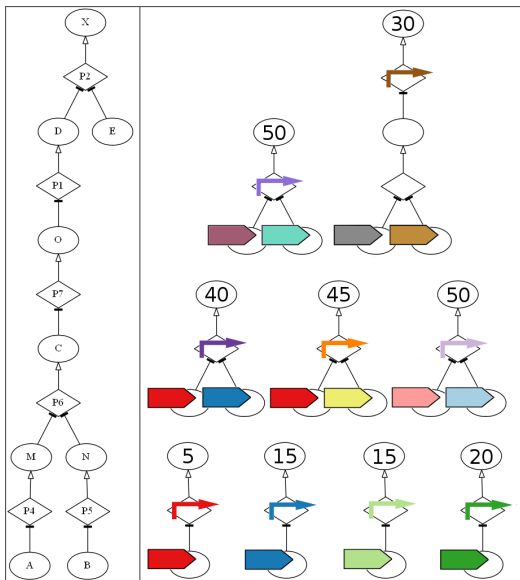
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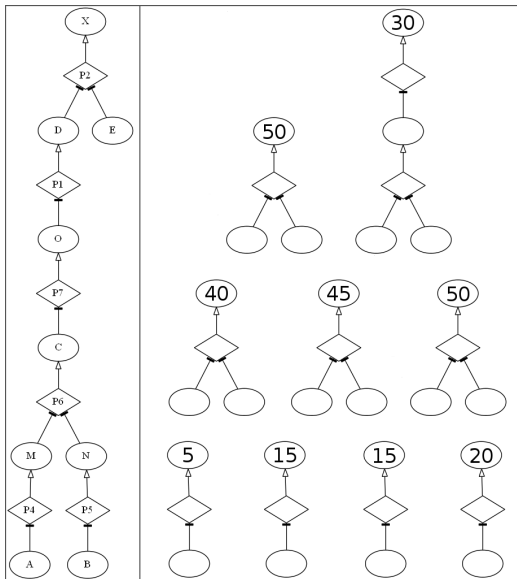
Matching



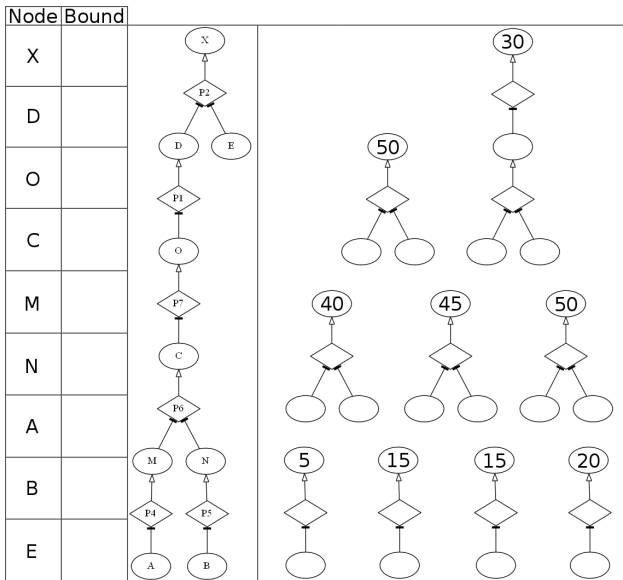
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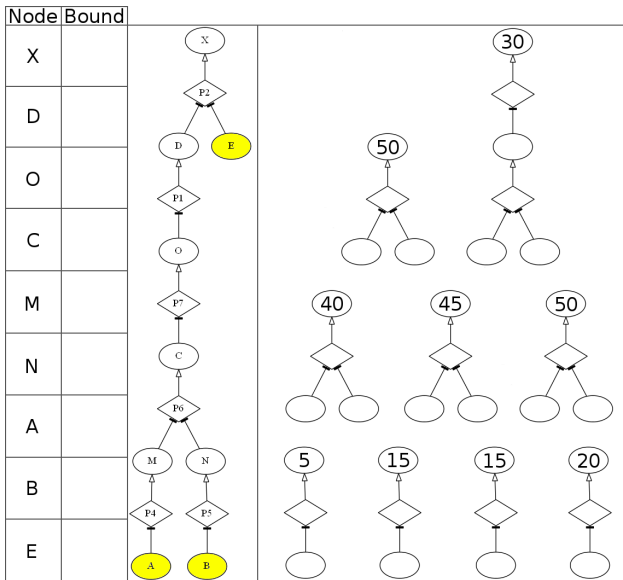
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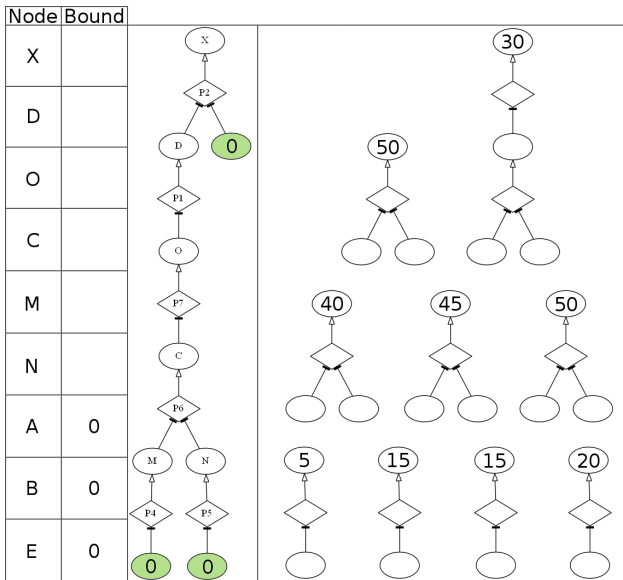
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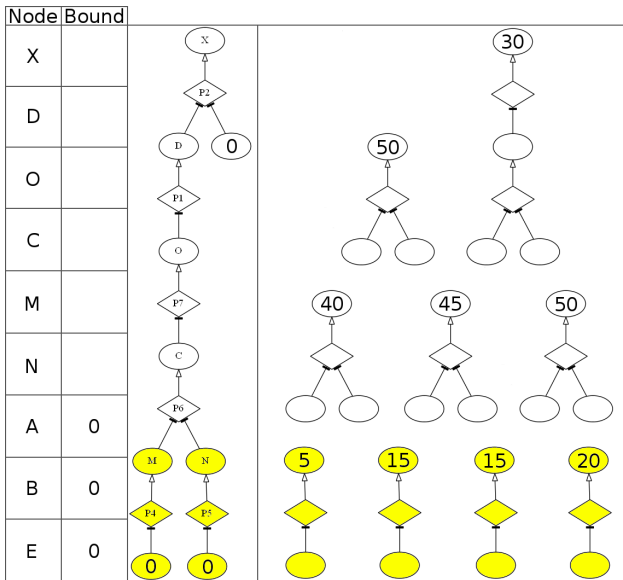
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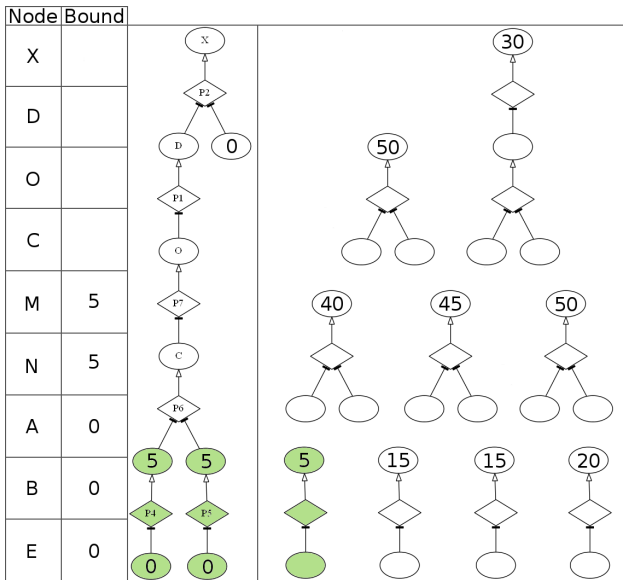
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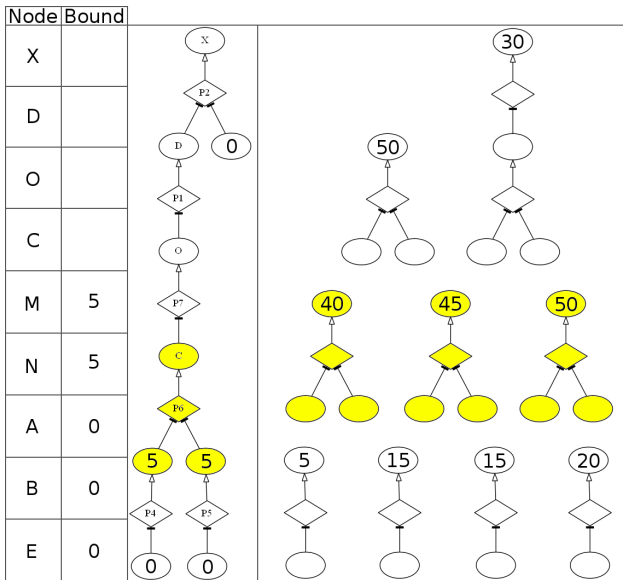
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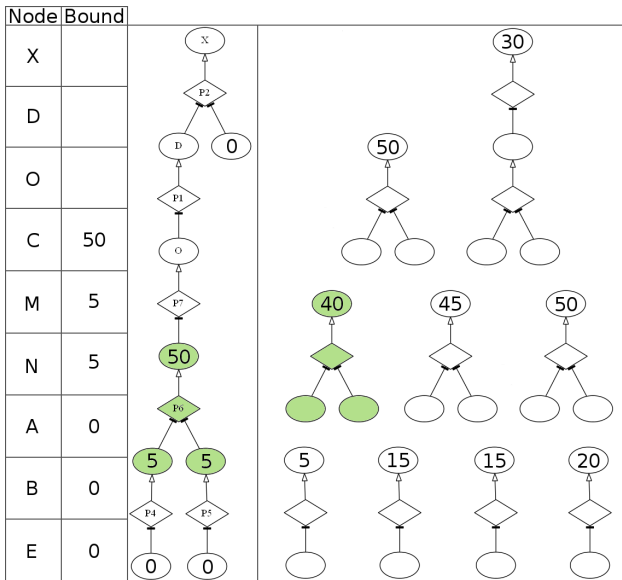
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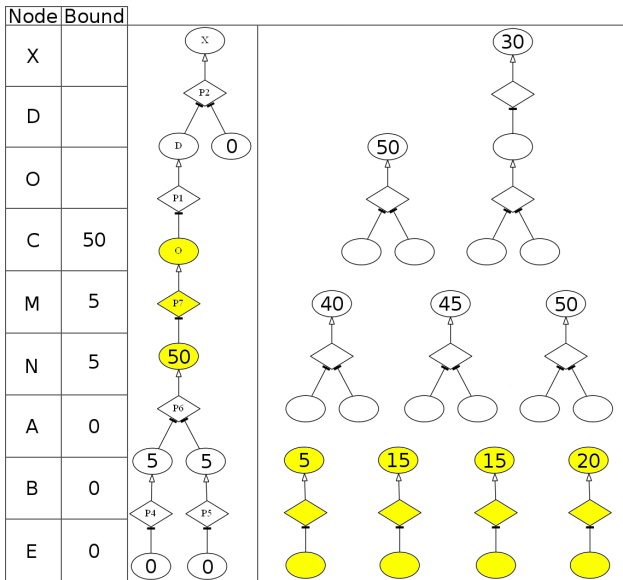
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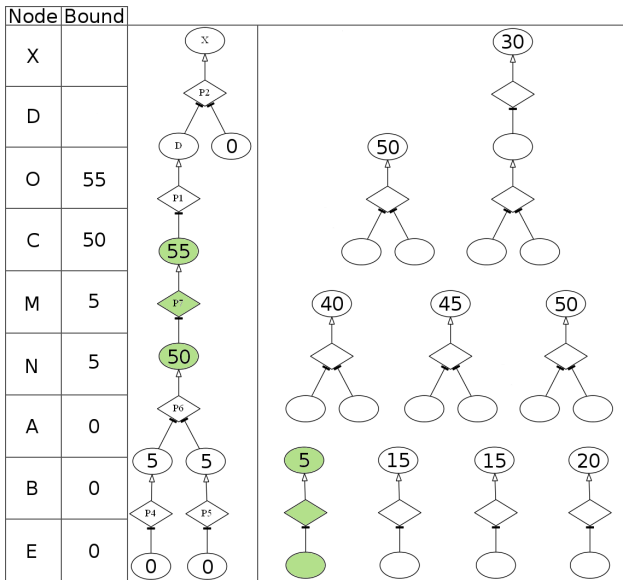
Matching



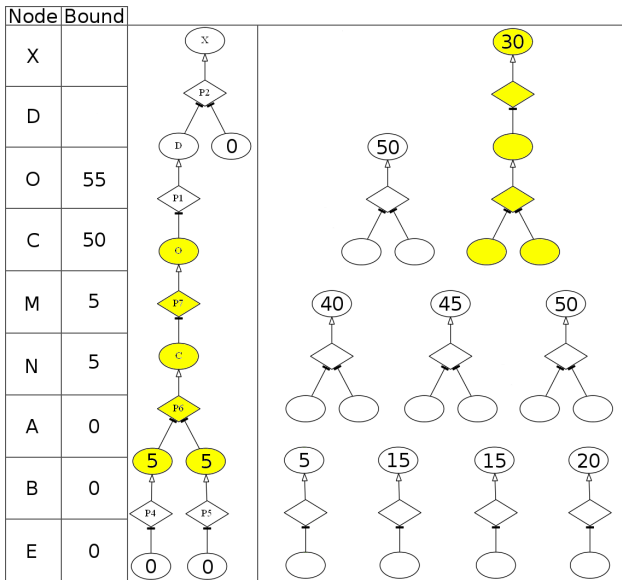
Matching



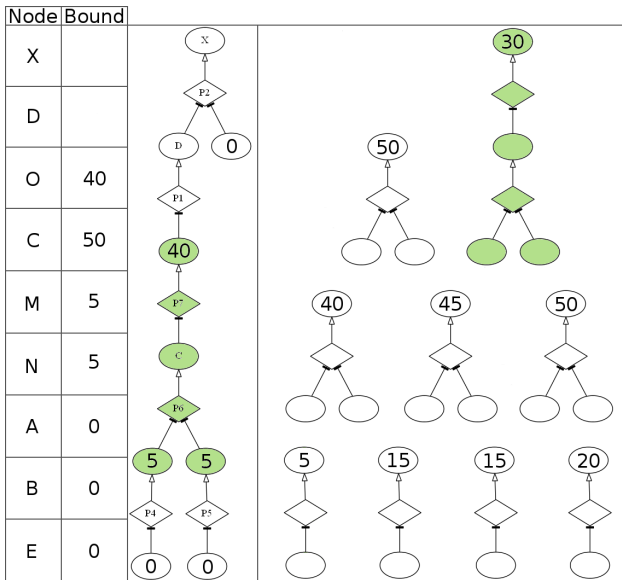
Matching



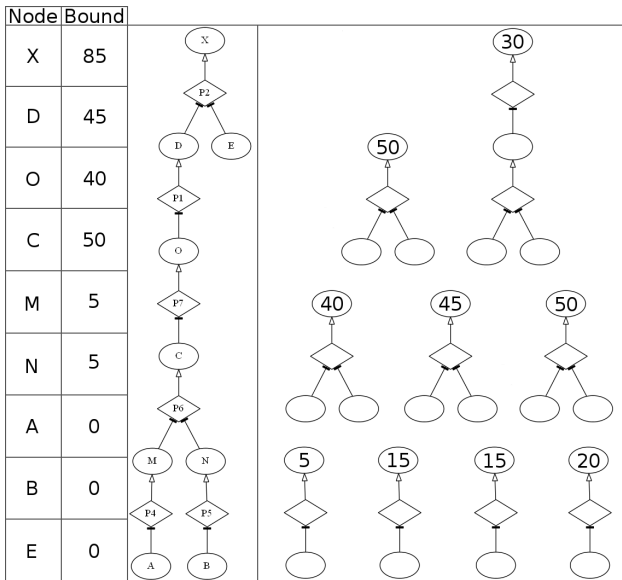
Matching



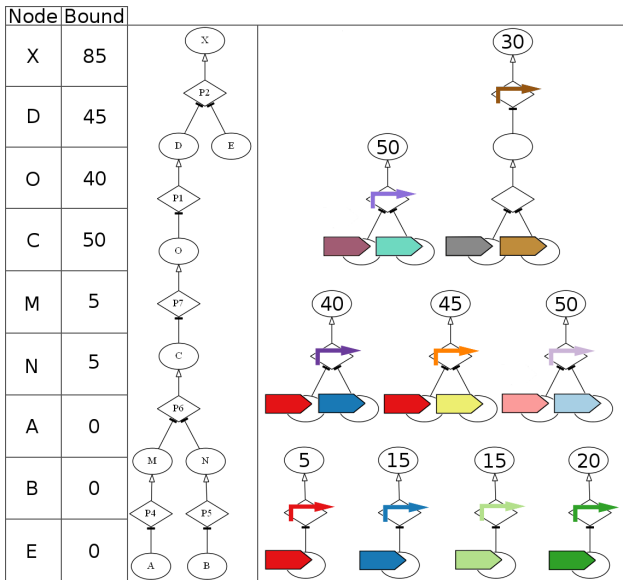
Matching



Matching

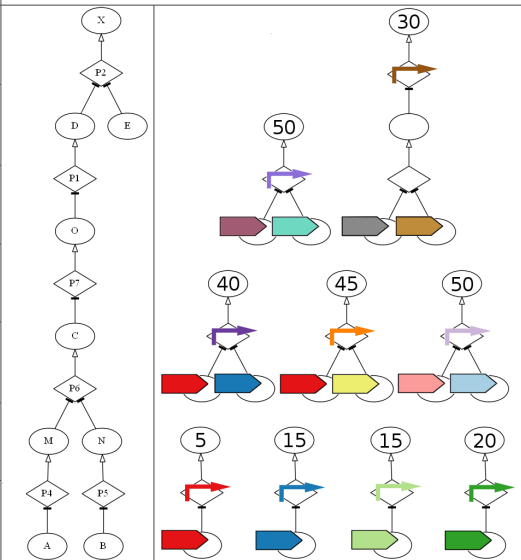


Covering



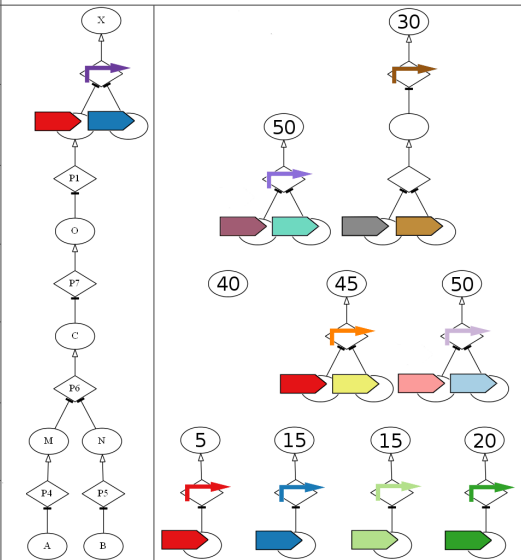
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E		45,0	
O		40	
C		50	
M,N		5,5	
A,N		0,5	
B		0	



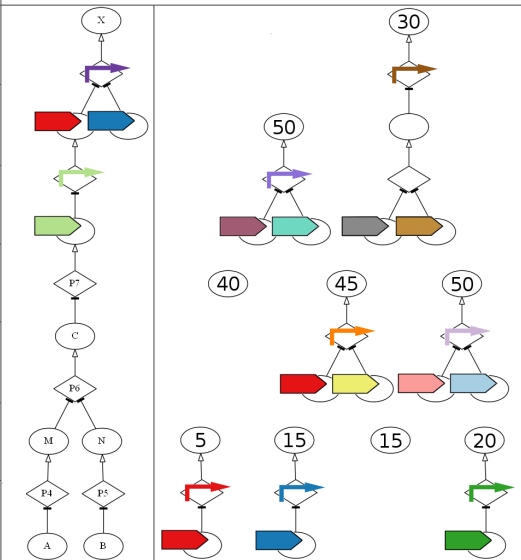
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E	40	45,0	85
O		40	
C		50	
M,N		5,5	
A,N		0,5	
B		0	



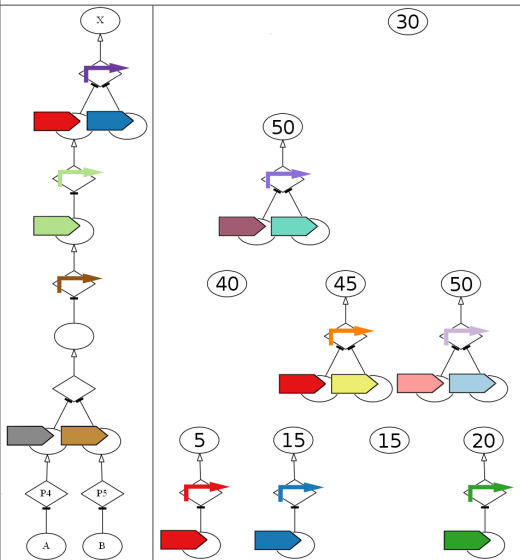
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E	40	45,0	85
O	55	40	95
C		50	
M,N		5,5	
A,N		0,5	
B		0	



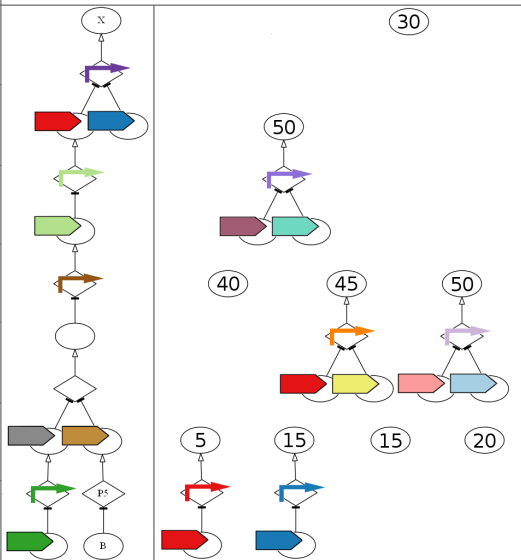
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E	40	45,0	85
O	55	40	95
C	-	50	-
M,N	85	5,5	95
A,N		0,5	
B		0	



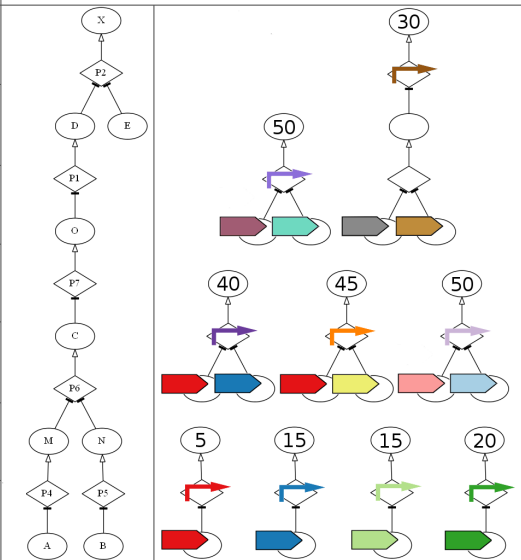
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E	40	45,0	85
O	55	40	95
C	-	50	-
M,N	85	5,5	95
A,N	105	0,5	110
B		0	



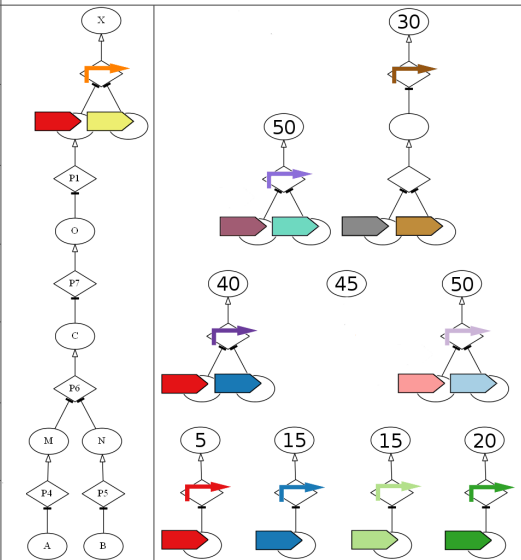
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E		45,0	
O		40	
C		50	
M,N		5,5	
A,N		0,5	
B		0	



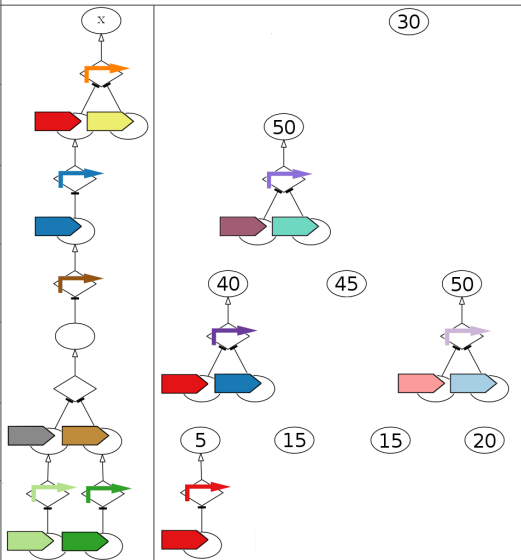
Covering

Node	Current	Bound	Estimate
X	0	85	85
D,E	45	45,0	90
O		40	
C		50	
M,N		5,5	
A,N		0,5	
B		0	

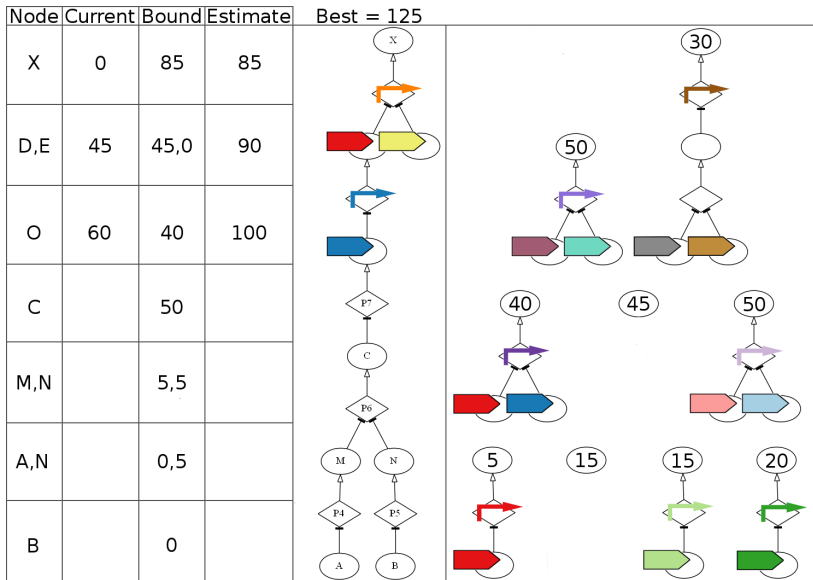


Covering

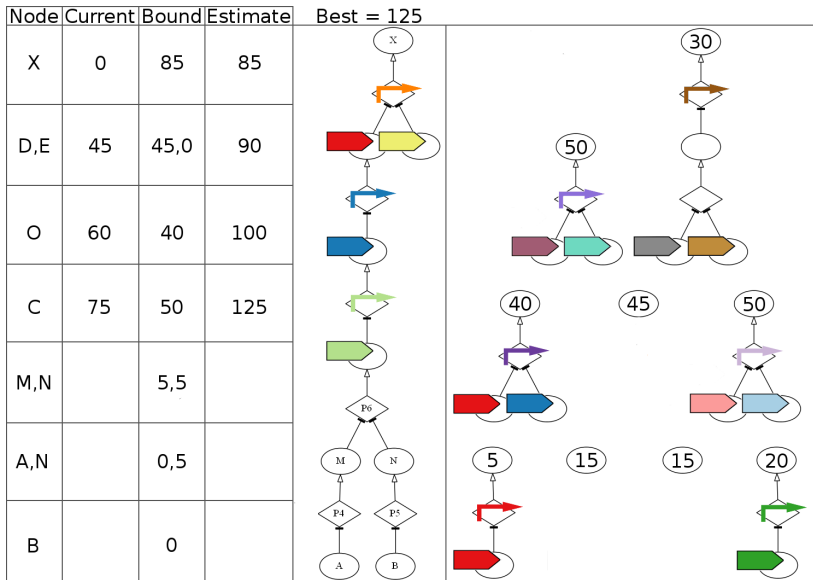
Node	Current	Bound	Estimate
X	0	85	85
D,E	45	45,0	90
O	60	40	100
C	-	50	-
M,N	90	5,5	100
A,N	105	0,5	110
B	125	0	125



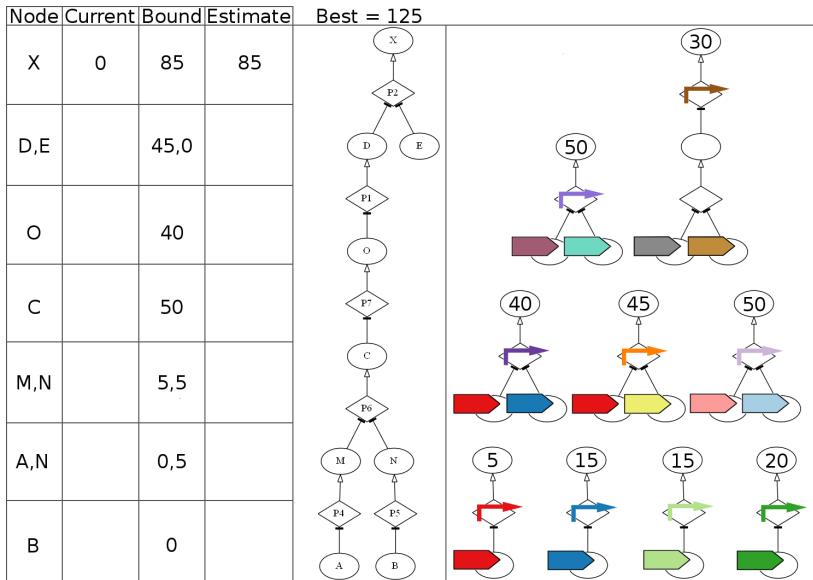
Covering



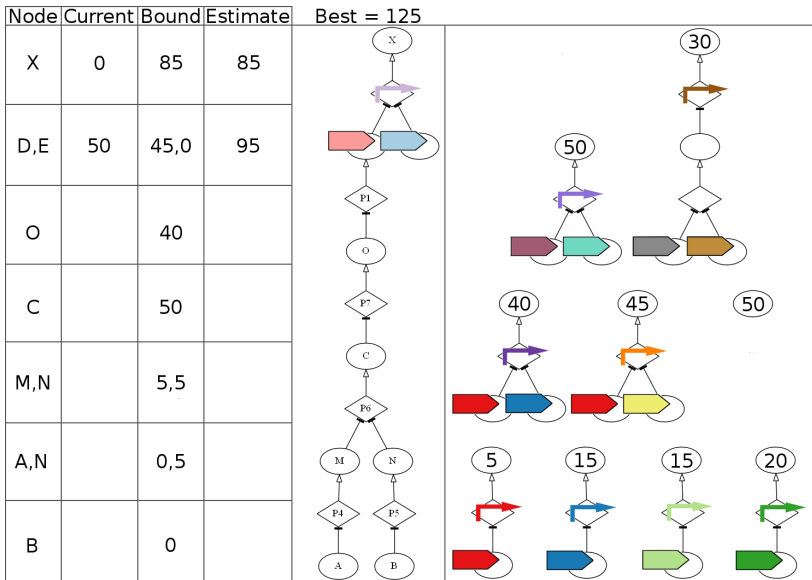
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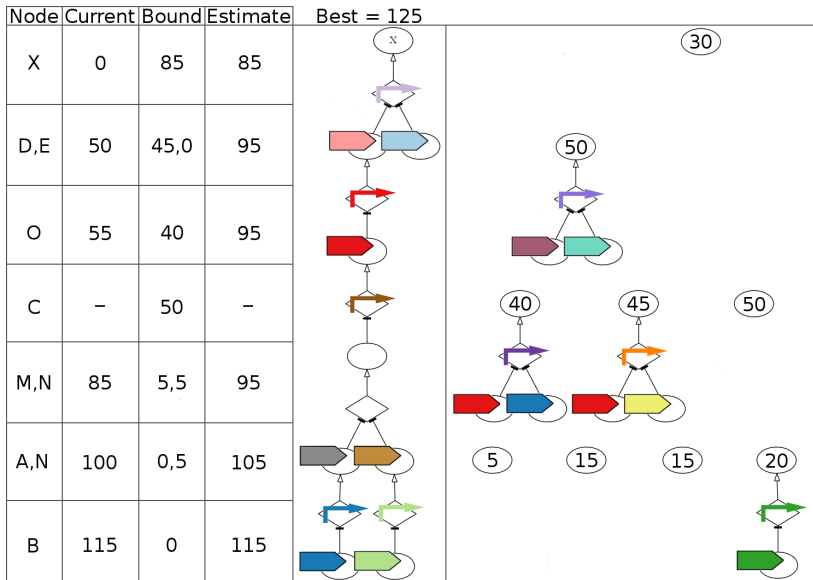
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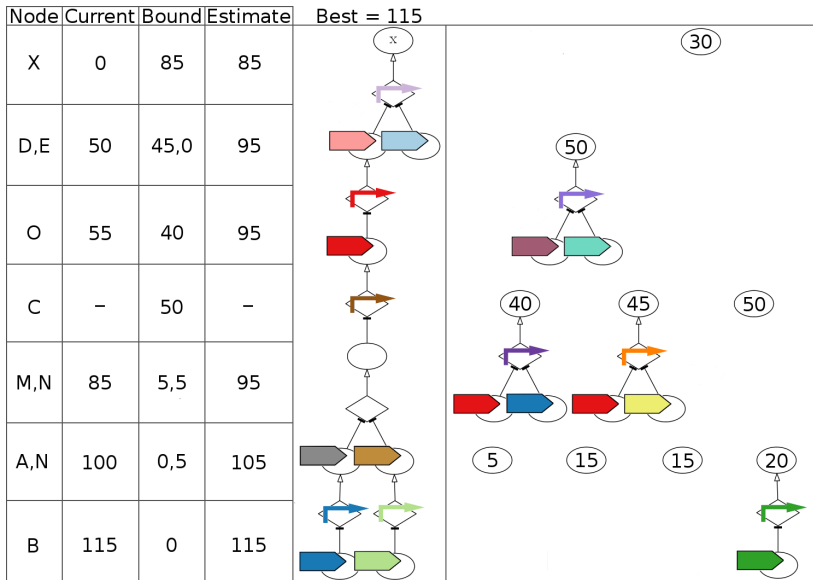
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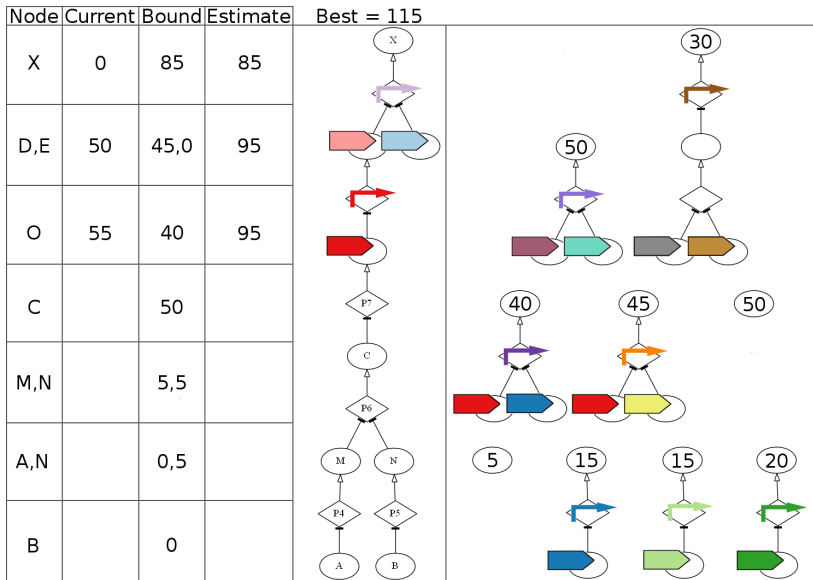
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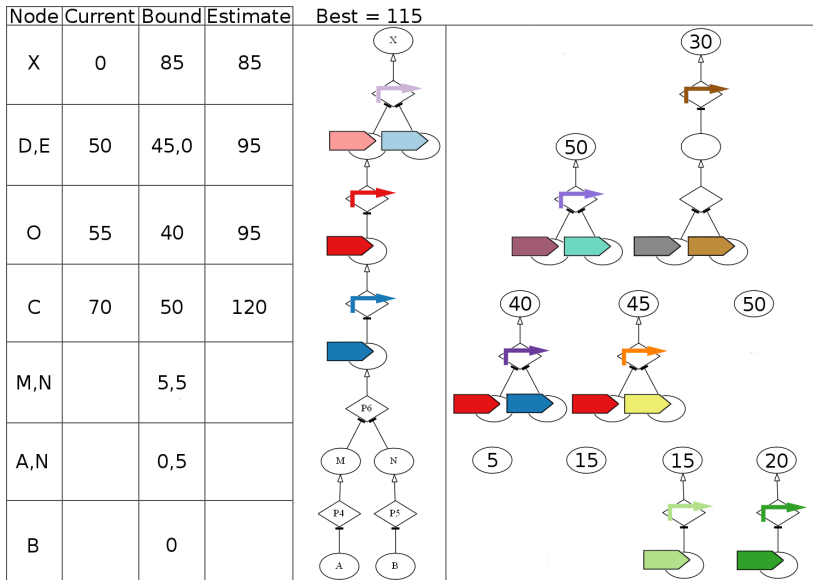
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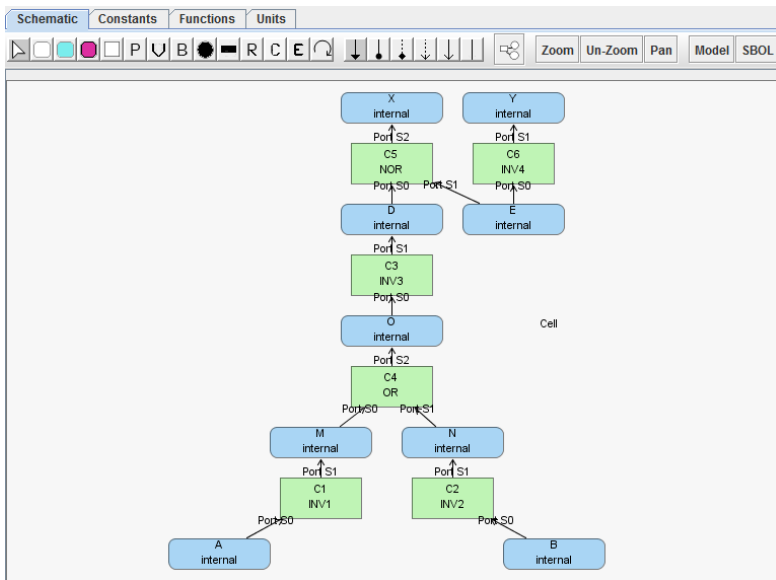
Covering



Covering



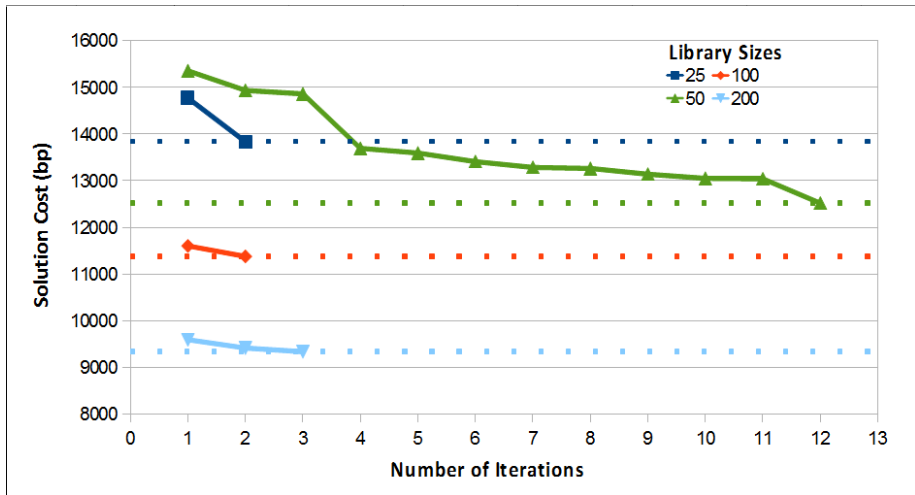
Output Design in iBioSim



Solution Cost Versus Iteration for OAI Circuit

AOI	Runtime (s)				Solution Cost (bp)			
Algorithm	Library Size				Library Size			
	25	50	100	200	25	50	100	200
Exhaustive	0.2	1	60	>1h	3662	2871	2946	n/a
Greedy	0.007	0.01	0.02	0.03	3662	2871	2946	2913
Branch/bound	0.008	0.01	0.02	0.03	3662	2871	2946	2913
NAND/NOR	Runtime (s)				Solution Cost (bp)			
Algorithm	Library Size				Library Size			
	25	50	100	200	25	50	100	200
Exhaustive	1	>1h	>1h	>1h	11178	n/a	n/a	n/a
Greedy	0.02	0.03	0.04	0.06	13219	10933	11107	8482
Branch/bound	0.2	1	0.7	1	11178	10931	10592	8270
OAI Cascade	Runtime (s)				Solution Cost (bp)			
Algorithm	Library Size				Library Size			
	25	50	100	200	25	50	100	200
Exhaustive	>1h	>1h	>1h	>1h	n/a	n/a	n/a	n/a
Greedy	2	0.03	0.04	0.07	14774	15357	11603	9592
Branch/bound	4	100	10	40	13836	12518	11377	9335

Solution Cost Versus Iteration for OAI Circuit

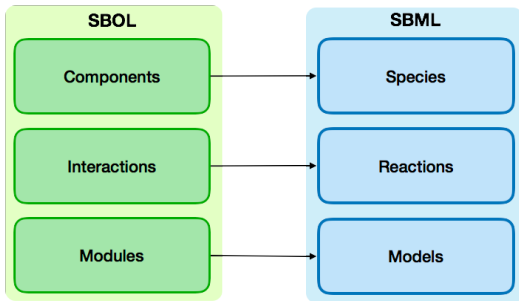


Verification

- Large amount of information is being produced about biological parts that can be used to build complex designs.
- Computational modeling *in silico* are created manually to predict the behavior of designs implemented *in vivo* or *in vitro*.
- Models in these designs have functional relationships and design constraints between parts that can be used for simulation.
- Computational models can be created by extracting knowledge about the DNA components and their interacting entities.
- These models can then be used to create simulations to verify performance of genetic circuit.

Deriving Dynamic Models

- SBOL to SBML conversion is applied to verify the behavior of a design.
- Ontology terms are used to translate components between standards.

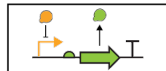
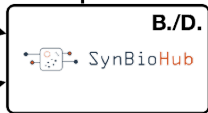


Model Generation Workflow

7,744 DNA Parts
4,189 Proteins
510 Complexes
4,853 Interactions



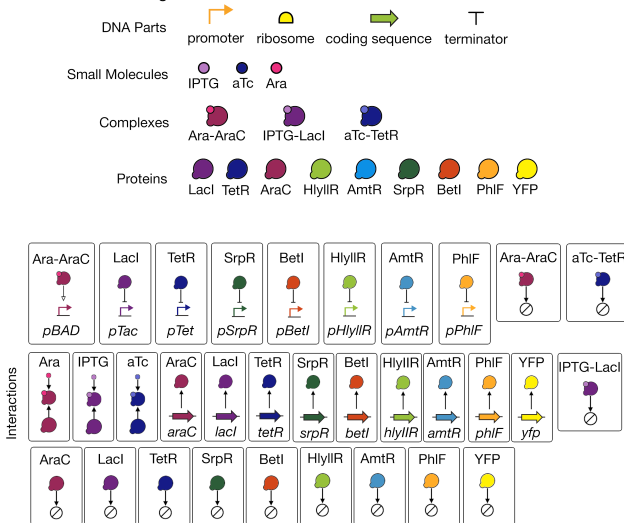
121 DNA Parts
17 Proteins
4 Complexes
58 Interactions



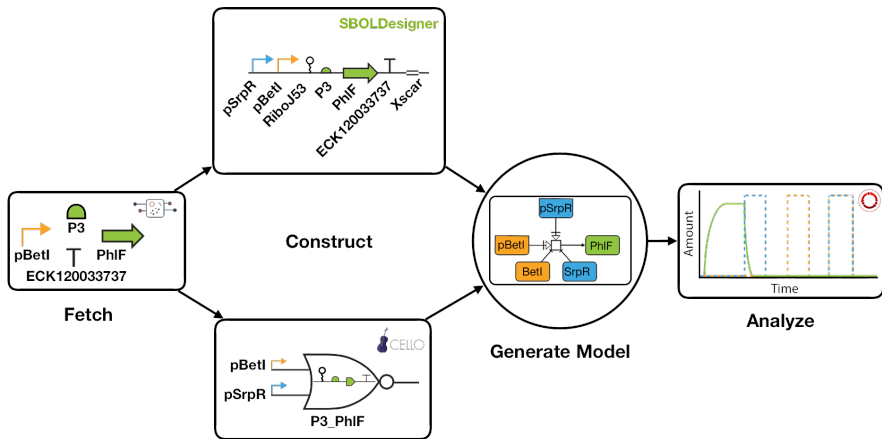
Mısırlı et al., *ACS Synthetic Biology* (2018).

Data Integration: Cello Part Library

A. Data Integration

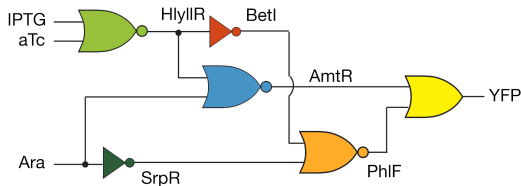


Genetic Circuit Construction

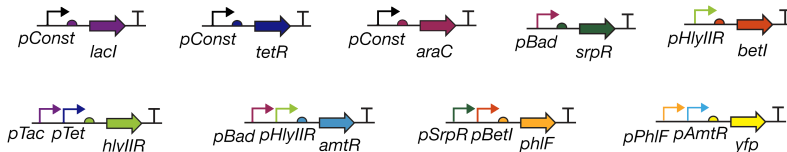


Genetic Circuit Construction: Rule 30 Example

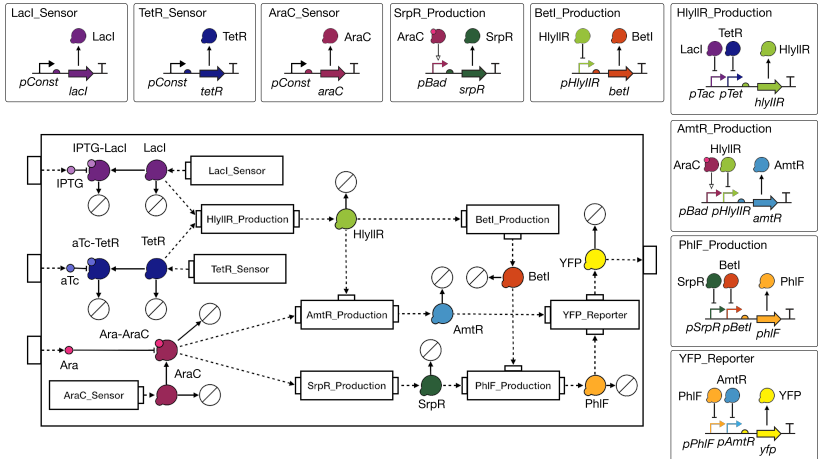
B. Rule 30



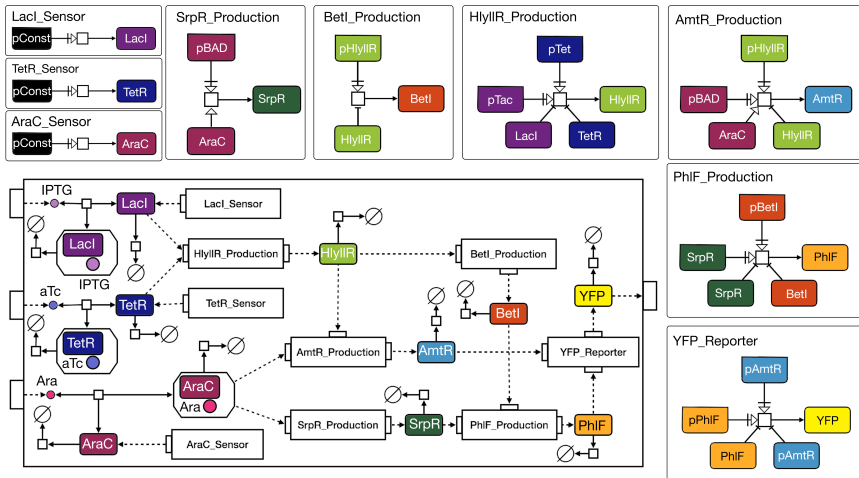
C. Genetic Circuit Construction



Enriched SBOL Representation: Rule 30 Example

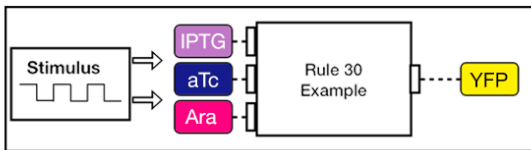


Dynamic SBML Model: Rule 30 Example

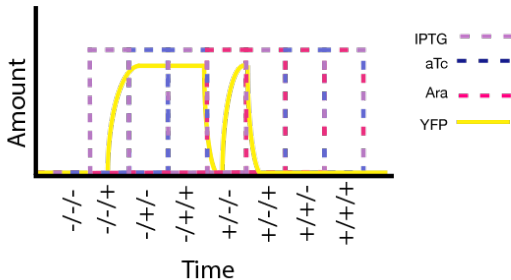


Simulation: Rule 30 Example

A. Testing Environment



B. Simulation



Sequential Genetic Circuits

- Existing frameworks are limited to combinational circuits.
- Memory circuits have been created but have not been introduced to technology mapping tools.
- The impact of designing genetic circuits sequentially needs to be explored on a deeper level.

Synchronous and Asynchronous Designs

- Sequential circuits can be designed synchronously or asynchronously.
- **Synchronous designs** use a global clock signal to order operations.
- **Asynchronous designs** order operations using handshaking protocols.
- Biological systems are naturally asynchronous.

Synchronous Genetic Sensor Example

```
module sync_sensor(Clock, Sensor, Actuator);  
    input Clock, Sensor;  
    output reg Actuator;  
    initial begin  
        Actuator = 1'b0;  
    end  
    always @(posedge Clock) begin  
        Actuator = Sensor;  
    end  
endmodule
```

Asynchronous Genetic Sensor Example

```
module async_sensor(Start, Sensor, Actuator);  
    input wire Start, Sensor;  
    output reg Actuator;  
initial begin  
    Actuator = 1'b0;  
end  
always begin  
    wait (Start == 1'b1 && Sensor == 1'b1);  
    #5 Actuator = 1'b1;  
    wait (Sensor == 1'b0);  
    #5 Actuator = 1'b0;  
end  
endmodule
```

Asynchronous Genetic Design Workflow

Synthesis

```
module srlatch(IPTG, aTc, GFP);
output reg GFP;
input wire IPTG, aTc;

assign GFP = (IPTG) | (~aTc) & GFP;

endmodule
```

ATACS

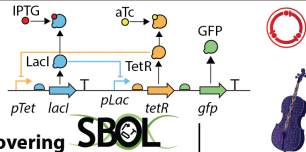
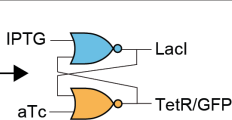
```
module srlatch(IPTG, aTc, GFP);
output reg GFP;
input wire IPTG, aTc;

initial begin
GFP = 1'b0;
end

always begin
wait (IPTG == 1'b1) #5;
#5 GFP = 1'b1;
wait (aTc == 1'b1) #5;
#5 GFP = 1'b0;
end
endmodule
```

Verilog

Technology Mapping



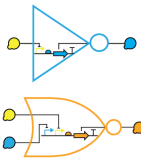
Matching & Covering



Library

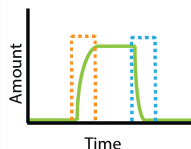


Parts Repository



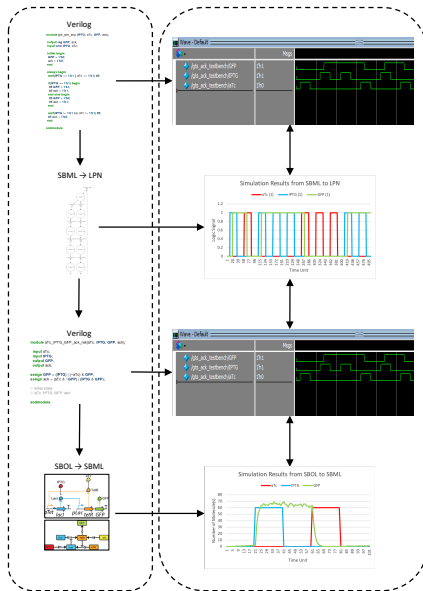
Gate Generation

Verification

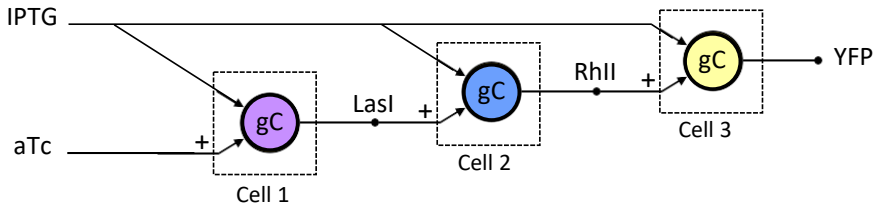


Model & Simulation

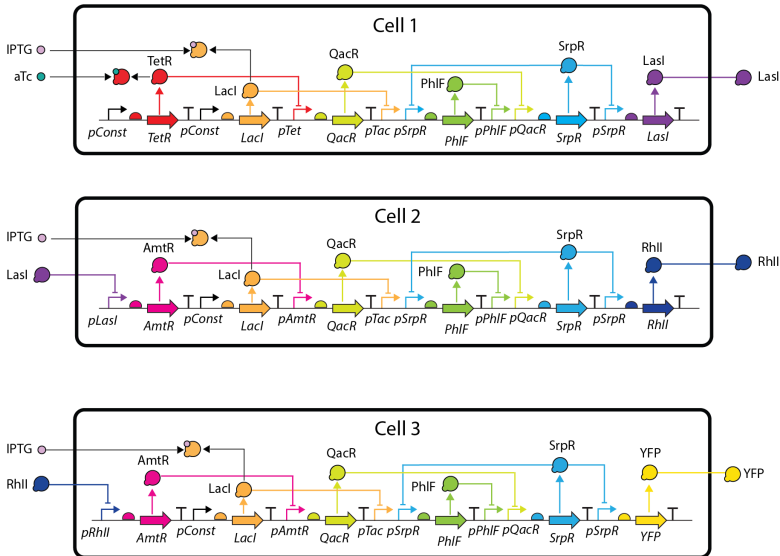
Verification Process



Genetic Sensor Design



Genetic Sensor Design



Future Work

- Asynchronous genetic circuit design workflow needs to be fully automated and seamless.
- Verilog templates should be developed to help designers who are not familiar with Verilog and/or asynchronous design.
- Hazards (i.e. unintended signal changes) in asynchronous genetic circuits should be more carefully considered and evaluated.
- Some asynchronous genetic designs produced by this workflow should be built and tested in the laboratory.