# Asynchronous Circuit Design

#### Chris J. Myers

Lecture 1: Introduction Preface and Chapter 1

# Synchronous Systems

• All events are synchronized to a single global clock.



# Synchronous Advantages

- Simple way to implement sequencing.
- Widely taught and understood.
- Available components.
- Simple way to deal with noise and hazards.

## Synchronous Disadvantages

- Clock distribution is difficult due to *clock skew*.
- Worst-case design.
- Sensitive to variations in physical parameters.
- Not modular.
- Power consumption.

#### • Synchronization is achieved without a global clock.













Global synchrony doesn't exist anyway

0



- Intrinsic elegance
- Global synchrony doesn't exist anyway

0 2 3 4 5 6 Easier to exploit concurrency 8 Intellectual challenge

- Intrinsic elegance
- Global synchrony doesn't exist anyway



- Intrinsic elegance
- Global synchrony doesn't exist anyway

- Metastability has time to end
  Avoid clock distribution costs
  Easier to exploit concurrency
  Intellectual challenge
- Intrinsic elegance
- Global synchrony doesn't exist anyway

- 1 2
- 3
- No clock alignment at the interfaces
- Metastability has time to end
- Avoid clock distribution costs
- Easier to exploit concurrency
- Intellectual challenge
- Intrinsic elegance
- Global synchrony doesn't exist anyway

- Ease of modular composition
- No clock alignment at the interfaces
- Metastability has time to end
- Avoid clock distribution costs
- Easier to exploit concurrency
- Intellectual challenge
- Intrinsic elegance
- Global synchrony doesn't exist anyway

- Power consumed only where needed
- Ease of modular composition
- No clock alignment at the interfaces
- Metastability has time to end
- Avoid clock distribution costs
- Easier to exploit concurrency
- Intellectual challenge
- Intrinsic elegance
- Global synchrony doesn't exist anyway

- Achieve average case performance
- Power consumed only where needed
- Ease of modular composition
- No clock alignment at the interfaces
- Metastability has time to end
- Avoid clock distribution costs
- Easier to exploit concurrency
- Intellectual challenge
- Intrinsic elegance
- Global synchrony doesn't exist anyway





It's none of your business

- •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •
  •<
- Olock radiation causes hair loss
- It's none of your business

- 0
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

- World problems stem from glitches
- Synchronous design gives me gas
- Olock radiation causes hair loss
- It's none of your business

- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Olock radiation causes hair loss
- It's none of your business

- 0 2
- 3

- People and circuits need to play by the same rules
- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

- 0 2
- 3
- Gee I really don't know
- People and circuits need to play by the same rules
- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

- I like to be different
- Gee I really don't know
- People and circuits need to play by the same rules
- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

- I like reinventing wheels
- I like to be different
- Gee I really don't know
- People and circuits need to play by the same rules
- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

- It really pisses my boss off
- I like reinventing wheels
- I like to be different
- Gee I really don't know
- People and circuits need to play by the same rules
- I don't understand synchronous circuits
- World problems stem from glitches
- Synchronous design gives me gas
- Clock radiation causes hair loss
- It's none of your business

# Asynchronous Challenges

- Lack of mature computer-aided design tools.
- Large area overhead for the removal of hazards.
- Average-case delay can be large.
- Lack of designer experience.

## Asynchronous Circuit History

- Every design method traces its roots to one of two individuals:
  - Huffman fundamental-mode circuits.
  - Muller speed-independent circuits.

### Key Asynchronous Circuit Designs

- ILLIAC (1952) and ILLAC2 (1962) U. of Illinois
- Atlas (1962) and MU-5 (1966) U. of Manchester
- Macromodules (60s-70s) Washington U., St. Louis
- First commercial graphics system (70s) Evans & Sutherland
- DDM dataflow computer (1978) U. of Utah
- First asynchronous microprocessor (1989) Caltech
- First code-compatible processor (1994) U. of Manchester
- Commercial pager (90s) Phillips
- RAPPID (1995-9) Intel

### Asynchronous Startups

- Handshake Solutions Microcontrollers (Phillips)
- Fulcrum Ethernet Switches (Caltech)
- Silistix Self-timed interconnect (U. of Manchester)
- Achronix Semiconductor Asynchronous FPGAs (Cornell)

## Asynchronous Startups

- Handshake Solutions Microcontrollers (Phillips)
- Fulcrum Ethernet Switches (Caltech) ← acquired by Intel
- Silistix Self-timed interconnect (U. of Manchester)
- Achronix Semiconductor Asynchronous FPGAs (Cornell) ← founder left

### Wine Shop Problem Specification

- Small winery and wine shop in Southern Utah.
- Only a single wine patron.
- Wine shop only has a single small shelf.
- Synchronous versus asynchronous wine shopping.

### **Channels of Communication**



### Channels of Communication in VHDL

# Winery:process

### begin

send(WineryShop, bottle);

### end process;

### Shop:process

### begin

receive(WineryShop,shelf); send(ShopPatron,shelf);

### end process;

Patron: process

### begin

receive(ShopPatron,bag);

### end process;

### **Event Protocol**

### Shop:process begin

req\_wine; - call winery
ack\_wine; - wine arrives
req\_patron; - call patron
ack\_patron; - patron buys wine

#### end process;
#### Shop:process begin

assign(req\_wine,'1'); - call winery
guard(ack\_wine,'1'); - wine arrives
assign(req\_patron,'1'); - call patron
guard(ack\_patron,'1'); - patron buys wine
end process;

#### 2-Phase Protocol

# Shop\_2Phase:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_wine,'0'); - call winery guard(ack\_wine,'0'); - wine arrives assign(req\_patron,'0'); - call patron guard(ack\_patron,'0'); - patron buys wine end process;

#### Waveform for 2-Phase Protocol



## Shop\_4Phase:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_wine,'0'); - reset req\_wine guard(ack\_wine,'0'); - ack\_wine resets assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

#### Waveform for 4-Phase Protocol



guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

#### 4-Phase Protocol: Passive/Passive

#### 4-Phase Protocol: Passive/Passive

Shop\_PP:process

#### 4-Phase Protocol: Passive/Passive

Shop\_PP:process begin

guard(req\_wine,'1'); - winery calls

```
guard(req_wine,'1'); - winery calls
assign(ack_wine,'1'); - wine is received
```

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(req\_patron,'1'); - patron calls

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(req\_patron,'1'); - patron calls assign(ack\_patron,'1'); - sells wine

### Shop\_PP:process

### begin

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(req\_patron,'1'); - patron calls assign(ack\_patron,'1'); - sells wine guard(req\_patron,'0'); - req\_patron resets

### Shop\_PP:process

#### begin

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(req\_patron,'1'); - patron calls assign(ack\_patron,'1'); - sells wine guard(req\_patron,'0'); - req\_patron resets assign(ack\_patron,'0'); - reset ack\_patron end process;

#### Active/Active Protocol

# Shop\_AA:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_wine,'0'); - reset req\_wine guard(ack\_wine,'0'); - ack\_wine resets assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

#### Active/Active Protocol

# Shop\_AA:process begin

assign(req\_wine,'1'); - call winery
guard(ack\_wine,'1'); - wine arrives
assign(req\_wine,'0'); - reset req\_wine
guard(ack\_wine,'0'); - ack\_wine resets

 $\Rightarrow$  state coding problem here

assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

#### Active/Active Reshuffled

# Shop\_AA\_reshuffled:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_wine,'0'); - reset req\_wine guard(ack\_wine,'0'); - ack\_wine resets assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets

# Shop\_AA\_reshuffled:process begin

assign(req\_wine,'1'); guard(ack\_wine,'1'); assign(req\_patron,'1'); guard(ack\_patron,'1'); assign(req\_wine,'0'); guard(ack\_wine,'0'); assign(req\_patron,'0'); guard(ack\_patron,'0');











#### Karnaugh Maps for Huffman's A/A Reshuffled Circuit






















#### Active/Active Reshuffled Circuit



This circuit is *delay-insensitive*.

# Shop\_PA:process begin

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - wine is received guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

# Shop\_PA\_reshuffled:process begin

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - receives wine assign(req\_patron,'1'); - call patron guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

# Shop\_PA\_lazy\_active:process begin

guard(req\_wine,'1'); - winery calls assign(ack\_wine,'1'); - receives wine guard(ack\_patron,'0'); - ack\_patron resets assign(req\_patron,'1'); - call patron guard(req\_wine,'0'); - req\_wine resets assign(ack\_wine,'0'); - reset ack\_wine guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron end process;

## Petri-net (P/LA reshuffled)



## Petri-net (P/LA reshuffled)



## Petri-net (P/LA reshuffled)



# Labeled Petri Net (LPN) (P/LA reshuffled)

# Shop\_PA\_lazy\_active:process begin

guard(req\_wine,'1'); assign(ack\_wine,'1'); guard(ack\_patron,'0'); assign(req\_patron,'1'); guard(req\_wine,'0'); assign(ack\_wine,'0'); guard(ack\_patron,'1'); assign(req\_patron,'0');



# LPN (P/LA reshuffled)



#### From LPN to State Graph to Circuit



# State Graph for P/LA Reshuffled ( $\langle$ rw, ap, aw, rp angle)



Chris J. Myers (Lecture 1: Introduction)

# Karnaugh Maps for Passive/Lazy-Active Reshuffled

	re	req_wine/ack_patron				req_wine/ack_patron					
		00	01	11	10		00	01	11	10	
ook wino/	00	0	0	1	1	00	0	0	0	0	
ack_wille/	01	0	0	0	0	01	1	0	0	1	
ieq_pation	11	0	0	1	1	11	1	1	1	1	
	10	1	1	1	1	10	1	0	0	1	
ack wine				 reg patron							

Chris J. Myers (Lecture 1: Introduction)























This circuit is *delay-insensitive*.

## Active/Active Protocol

# Shop\_AA:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_wine,'0'); - reset req\_wine guard(ack\_wine,'0'); - ack\_wine resets assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

# Shop\_AA\_state\_variable:process begin

assign(req\_wine,'1'); - call winery quard(ack wine, '1'); - wine arrives assign(x, '1'); - set state variable assign(req\_wine,'0'); - reset req\_wine quard(ack wine, '0'); - ack wine resets assign(req\_patron,'1'); - call patron quard(ack patron, '1'); - patron buys wine assign(x, '0'); - reset state variable assign(req\_patron,'0'); - reset req\_patron quard(ack patron,'0'); - ack patron resets end process;





req\_wine+, ack\_wine+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+



req\_wine+, ack\_wine+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+ u1-, u2-, x-, u4+, u6-



req\_wine+, ack\_wine+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+ u1-, u2-, x-, u4+, u6req\_wine glitches!

# **Huffman Circuits**



David Huffman

- Bounded gate and wire delay model.
- Circuit does not need to be closed.
- Single-input change fundamental mode.
- One input changes → output changes → state changes.
- May need to add delay in fed back state variables.

## Active/Active Protocol

# Shop\_AA:process begin

assign(req\_wine,'1'); - call winery guard(ack\_wine,'1'); - wine arrives assign(req\_wine,'0'); - reset req\_wine guard(ack\_wine,'0'); - ack\_wine resets assign(req\_patron,'1'); - call patron guard(ack\_patron,'1'); - patron buys wine assign(req\_patron,'0'); - reset req\_patron guard(ack\_patron,'0'); - ack\_patron resets end process;

#### AFSM and Huffman Flow Table (A/A)



ack wine / ack patron 00 01 11 10 (0) 000 1, -0 \_ 1 (1) 102, -0\_ 2 3.0 -(2) 00\_ 3 (3) 01 0, 0 -

req\_wine / req\_patron

# Reduced AFSM and Huffman Flow Table (A/A)



ack\_wine / ack\_patron

	00	01	11	10
0	<b>()</b> 10	0) 00	_	1, -0
1	1) 01	0,0-	_	(1) 00

req\_wine / req\_patron

## Karnaugh Maps for Huffman's A/A Circuit

ack_wine/ack_patron						
x	00	01	11	10		
0	1	0	_	-		
1	0	0	_	0		

req\_wine

ack wine/ack patron

X	00	01	11	10
0	0	0	_	0
1	1	_	_	0

req\_patron

ack\_wine/ack\_patron

X	00	01	11	10
0	0	0		1
1	1	0	_	1

Х

#### Huffman's Active/Active Circuit



#### Huffman's Active/Active Circuit


## Huffman's Active/Active Circuit



req\_wine+, ack\_wine+, X+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+

x will not go low until after both u2- and u6- due to feedback delay assumption.

# Muller Circuits



David Muller

- Unbounded gate delay model.
- Wire delays are assumed to be negligible.
- Forks are assumed to be *isochronic*.
- Model called *speed-independent*.

#### Muller's Active/Active Circuit



### Muller's Active/Active Circuit



req\_wine+, ack\_wine+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+

# Muller's Active/Active Circuit



req\_wine+, ack\_wine+, x+, req\_wine-, ack\_wine-, req\_patron+, ack\_patron+ ack\_patron change felt at both x and req\_wine gates simultaneously due to isochronic fork assumption.

Asynchronous Circuit Design

# **Timed Wine Shop**

# Shop\_AA\_timed:process begin

```
assign(req_wine,'1',0,1); - call winery
assign(req_patron,'1',0,1); - call patron
- wine arrives and patron arrives
guard_and(ack_wine,'1',ack_patron,'1');
assign(req_wine,'0',0,1);
assign(req_patron,'0',0,1);
- wait for ack_wine and ack_patron to reset
guard_and(ack_wine,'0',ack_patron,'0');
end process;
```

#### winery:process

#### begin

```
guard(req_wine,'1'); - wine requested
assign(ack_wine,'1',2,3); - deliver wine
guard(req_wine,'0');
assign(ack_wine,'0',2,3);
```

#### end process;

#### patron:process

# begin

```
guard(req_patron,'1'); - shop called
assign(ack_patron,'1',5,inf); - buy wine
guard(req_patron,'0');
assign(ack_patron,'0',5,7);
```

#### end process;

#### LPN for Timed Wine Shop Example



#### LPN for Timed Wine Shop Example



# State Graph for Timed Wine Shop Example



State vector: (ack\_wine, ack\_patron, req\_wine, req\_patron)

#### Karnaugh Maps for Timed Circuit



req\_wine

req\_patron

# **Timed Circuit**



- *Cycle time* is the delay from when the patron gets one bottle of wine until he can get another.
- Assuming the timed circuit delays are uniformly distributed except that the patron is extremely unlikely to take more then 10 minutes, we obtain the following cycle times:
  - Muller and Huffman's circuits (A/A SV) 21.5 minutes
  - Original (A/A reshuffled) 20.6 minutes
  - Timed circuit 15.8 minutes

# Validation versus Verification

- Validation is simulation of interesting situations.
- Verification is exhaustive checks of all possible situations.
  - Can check that circuit *conforms* to the specification.
  - Can check that protocol has certain properties.

# Sample Properties

- The wine arrives before the patron:
  - Always(ack\_patron ⇒ ack\_wine)
- When the wine is requested, it eventually arrives:
  - req\_wine ⇒ Eventually(ack\_wine)

# Summary of Course Topics

- Communication Channels
- Communication Protocols
- Graphical Representations
- Huffman Circuits
- Muller Circuits
- Timed Circuits
- Verification
- Applications