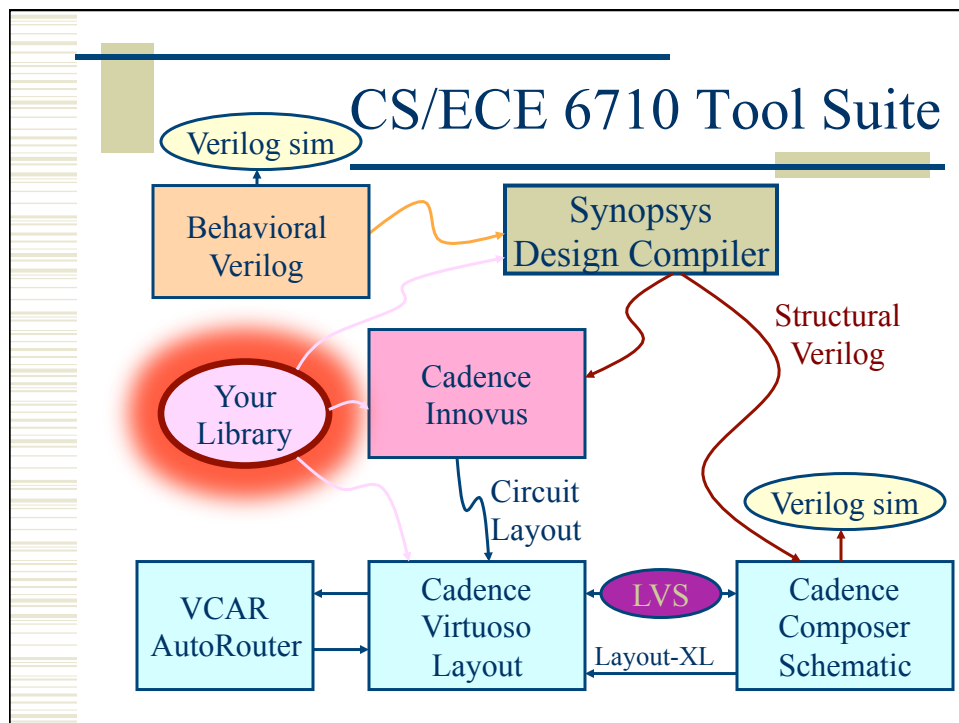


CAD5

- Designing the first five cells in your library
 - Multiple cell views
- Liberate library characterizer
- Abstract generator
- Synopsys database generation
 - Using the cells in synthesis

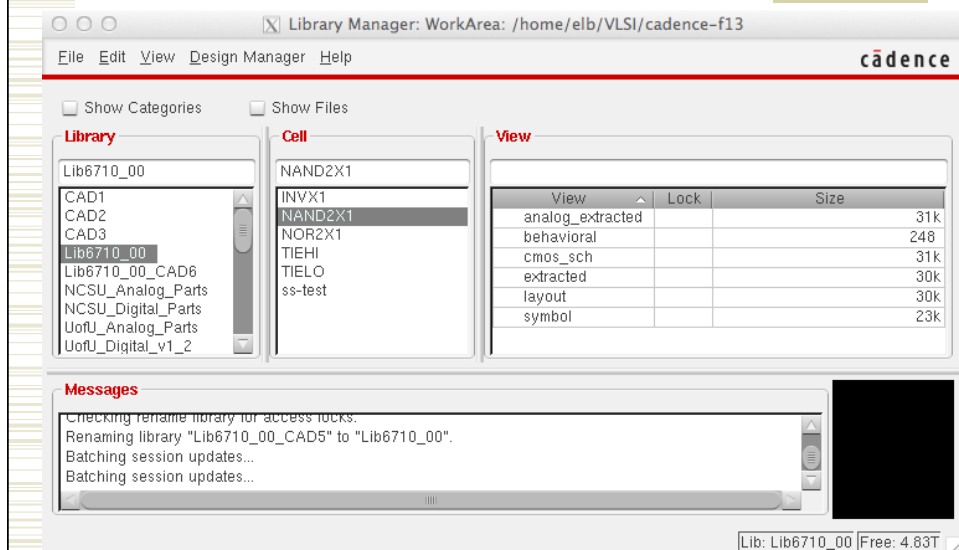


In the CAD Book

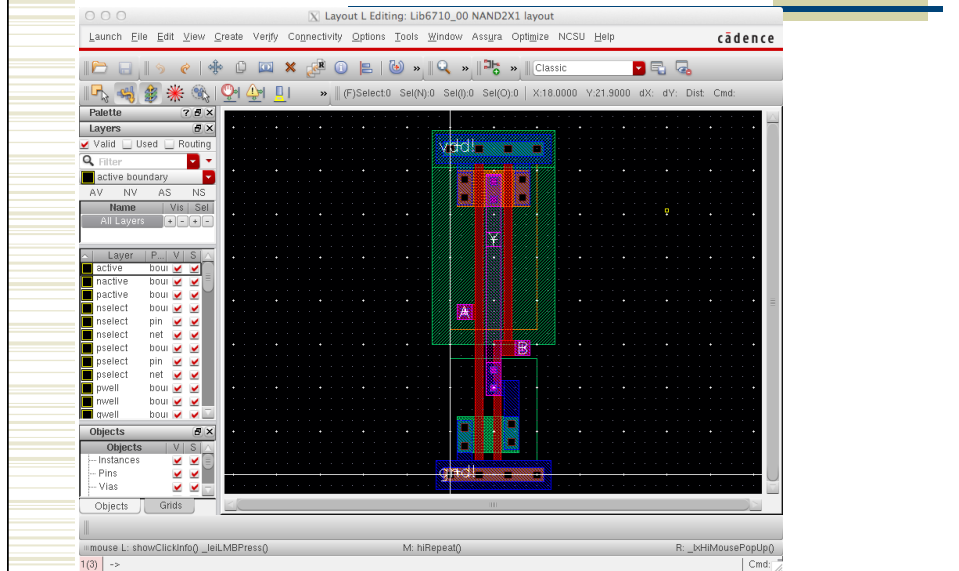
◆ Chapter 8 on Cell Characterization

- Section 8.1 describes .lib format
- Section 8.2 describes ELC – that tool is gone...
 - Instead we'll use Cadence Liberate
- Section 8.3 describes characterization by hand with Spectre (don't do it!)
- Section 8.4 describes converting from .lib to .db format (used by Synopsys Design Compiler)
 - Use syn-lc instead of syn-dc...
 - (.lib is used also by other tools...)

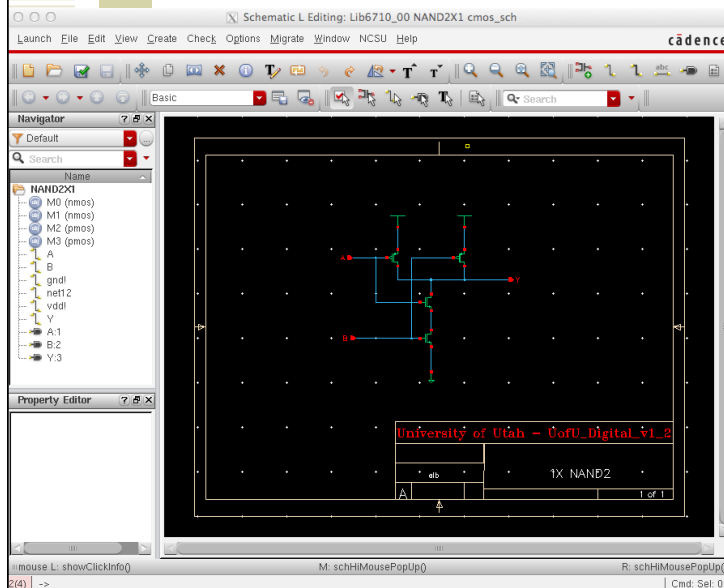
Start with Cells



Layout View



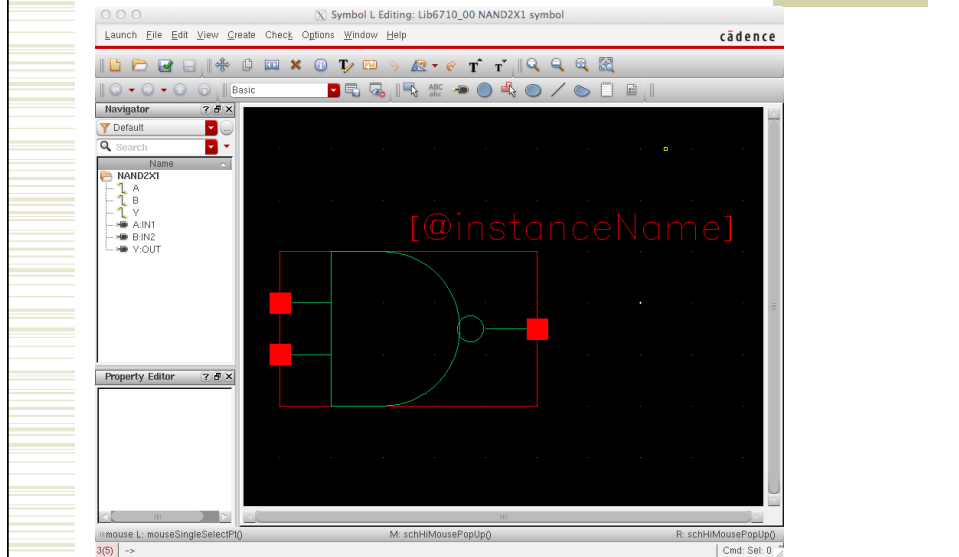
Schematic View



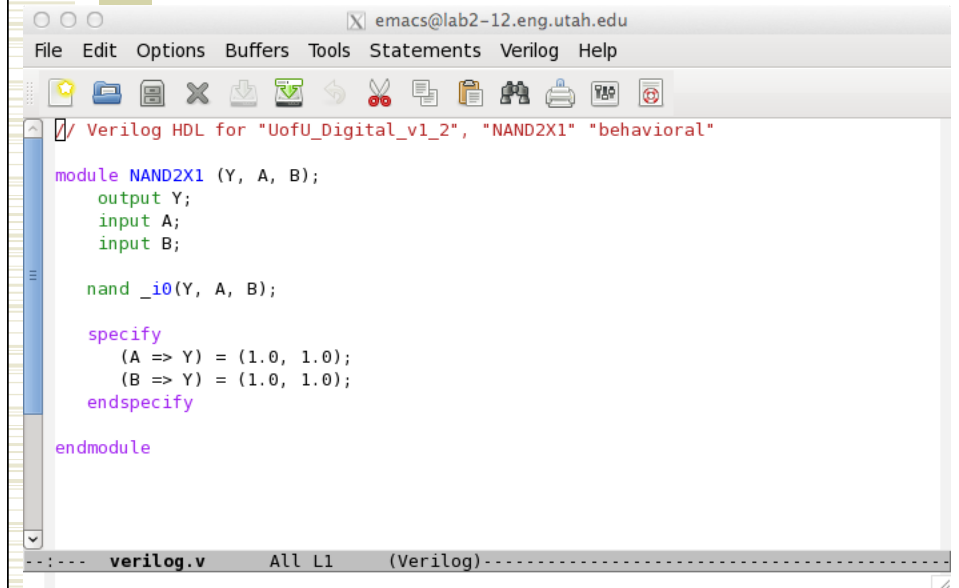
Use **cmos_sch** as the view type for your cell schematics

This is to differentiate them from schematics that use the cells.

Symbol View



Behavioral View



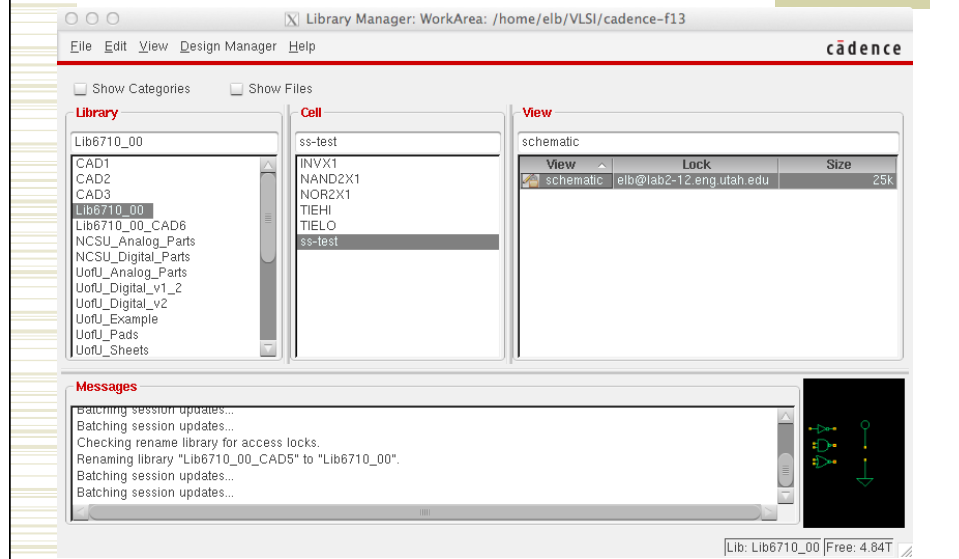
Start with six views of each cell

1. **layout** - make sure to use the template!
2. **cmos_sch** – use this view type for a schematic
3. **symbol** – Make them look nice
4. **behavioral** – Having this view makes simulation go much faster (if you use it)
5. **extracted** – generated from the extract processes
6. **analog_extracted** – after LVS

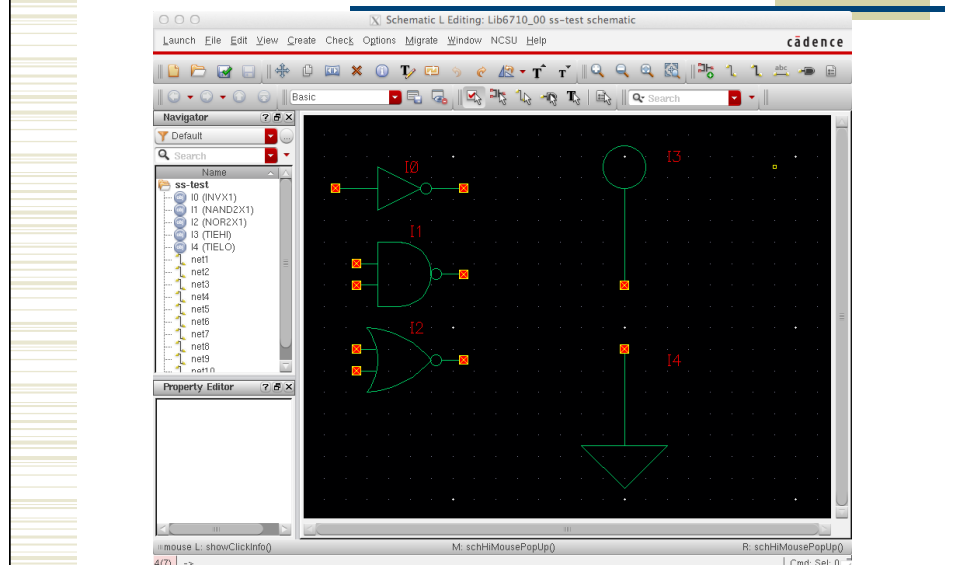
Characterize the cells

- ♦ Run a set of analog (Spectre) simulations that builds a table of delay values
 - Input drive vs. output load
 - For all outputs
 - Plus rise and fall times
 - And some power information
- ♦ Cadence Liberate
 - cad-lib from the bin directory
 - But, don't call it directly... use additional scripts...

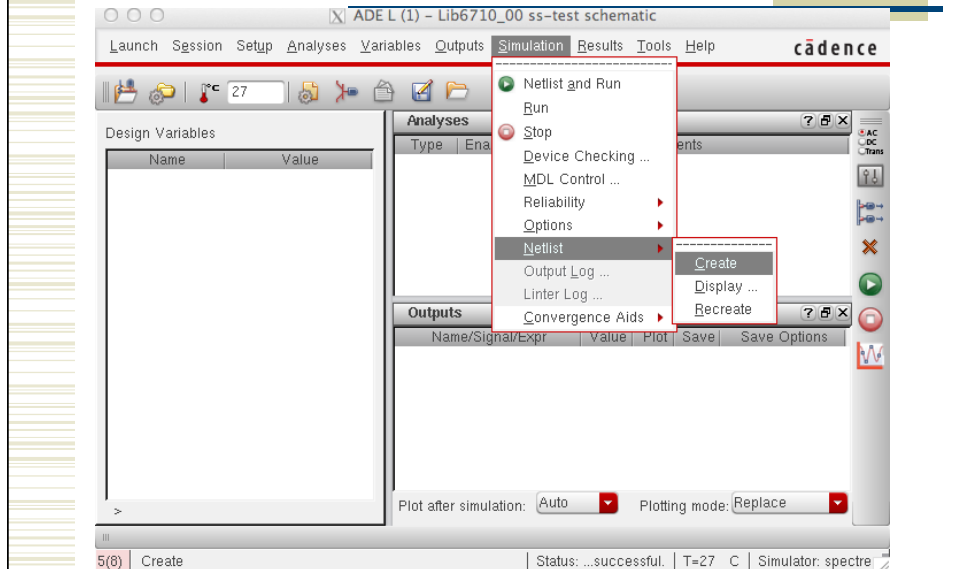
Single Schematic with All Cells



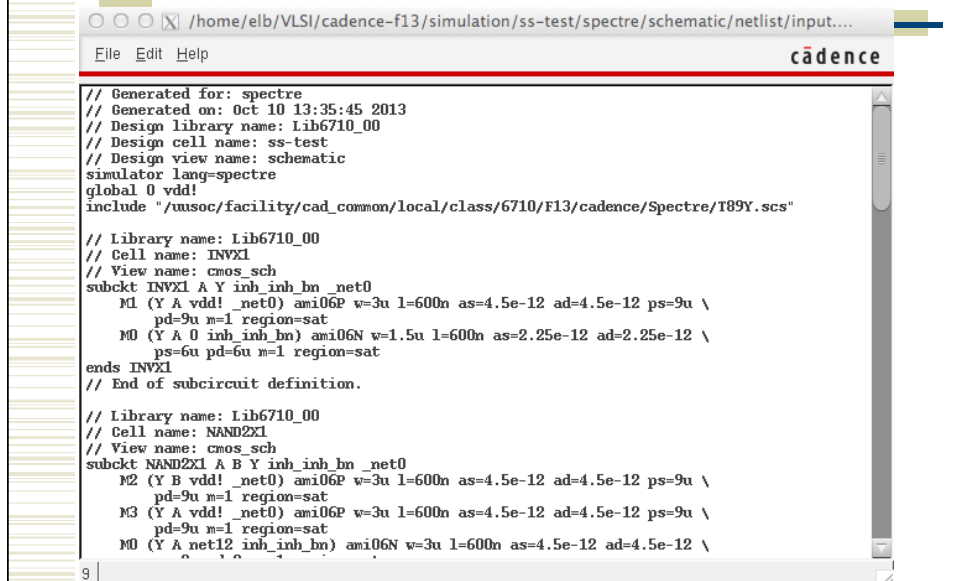
Single Schematic with All Cells



Create Netlist of that ss-test Cell



Call it foo.scs (for example)



Convert to Liberate format

```
simulator lang=spectre
global vss vdd

subckt INVX1 A Y
  M1 (Y A vdd vdd) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
    pd=15.0u m=1 region=sat
  M0 (Y A vss vss) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
    pd=9u m=1 region=sat
ends INVX1
subckt NAND2X1 A B Y
  M2 (Y A vdd vdd) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
    pd=15.0u m=1 region=sat
  M3 (Y B vdd vdd) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
    pd=15.0u m=1 region=sat
  M0 (Y B net12 vss) ami06N w=6u l=600n as=9e-12 ad=9e-12 \
    ps=15.0u pd=15.0u m=1 region=sat
  M1 (net12 A vss vss) ami06N w=6u l=600n as=9e-12 ad=9e-12 \
    ps=15.0u pd=15.0u m=1 region=sat
ends NAND2X1
```

Run Liberate

- ◆ Liberate Library Characterizer
 - Figures out what each cell is (logic)
 - Generates test inputs for Spectre
 - Runs Spectre
 - Checks output and extracts timings
 - Formats the output in .lib format
- ◆ I like to make a new VLSI/Liberate directory from which to run this tool...
 - `cp -r /uusoc/facility/cad_common/local/class/6710/F17/cadence/Liberate .`

Liberate setup...

- ♦ A **lib** directory
 - where the generated <library>.lib file will be generated.
- ♦ A **netlist** directory
 - put your **libcells.scs** file in this directory.

```
[elb@lab2-20 Liberate]$ ls
models/  README  tcl/      templates/  userdata/
netlist/  run.sh*  TechHeader.lef  UofU_Cells.tcl
[elb@lab2-20 Liberate]$
```

Liberate setup

- ♦ A **templates** directory
 - edit the **UofU_Cell_Defs.tcl** file in this directory to include cell descriptions for each of the cells you want to characterize. The **UofU_Templates.tcl** file has definitions for the timing and power templates that will be used for characterization. You probably don't need to modify these unless you are using a different technology than ON Semi C5N.

```
[elb@lab2-20 Liberate]$ ls
models/  README  tcl/      templates/  userdata/
netlist/  run.sh*  TechHeader.lef  UofU_Cells.tcl
[elb@lab2-20 Liberate]$
```

Liberate setup

♦ A UofU_Cells.tcl file

- edit this file to make a list of the cells that you want to characterize in this run. This could be a list of every cell described in **templates/UofU_Cell_Defs.tcl**, or it could be a subset if you just want to try a few.

♦ A userdata directory

- edit the **userdata.lib** file to reflect the areas and footprints of each of the cells in your library.

```
[elb@lab2-20 Liberate]$ ls
models/  README  tcl/      templates/  userdata/
netlist/  run.sh*  TechHeader.lef  UofU_Cells.tcl
[elb@lab2-20 Liberate]$
```

Liberate setup

♦ A tcl directory

- Edit the **UofU_Char.tcl** file in this directory to change the name of the library that the tool generates. If you don't modify this, the tool will generate a file named **Lib6710_XX.lib** by default. The **settings.tcl** file in this directory has configuration commands for the Spectre simulator. You won't need to modify this file at all.

```
[elb@lab2-20 Liberate]$ ls
models/  README  tcl/      templates/  userdata/
netlist/  run.sh*  TechHeader.lef  UofU_Cells.tcl
[elb@lab2-20 Liberate]$
```

Liberate setup

- ♦ A **models** directory
 - Has the Spectre model files for the ami06N and ami06P transistors used by in your netlist.
- ♦ A **run.sh** shell script
 - This calls the cad-lib Liberate script with the appropriate input files, and makes a copy of the log information in a **Liberate.log** file.

```
[elb@lab2-20 Liberate]$ ls
models/  README  tcl/          templates/  userdata/
netlist/ run.sh*  TechHeader.lef  UofU_Cells.tcl
[elb@lab2-20 Liberate]$
```

- ♦ **Liberate tutorial on Canvas...**

```
Terminal - ssh - 156x28
Sep 26 16:36:12 Thread 0: Cell=NAND2X1 (100%) Pin= Related= combinational leakage_power ...
Sep 26 16:36:12 Thread 0: Cell=NAND2X1 (100%) Pin= Related= combinational leakage_power ...
Performance statistics for NAND2X1: Spectre cpu time = 1.2 seconds, total cpu time = 1.3 seconds, wall clock time = 9.0 seconds.

Characterizing NOR2X1 (2)
Sep 26 16:36:12 Thread 0: Cell=NOR2X1 (20%) Pin=Y Related=A combinational rise_transition ...
Sep 26 16:36:12 Thread 0: Cell=NOR2X1 (41%) Pin=Y Related=B combinational rise_transition ...
Sep 26 16:36:12 Thread 0: Cell=NOR2X1 (62%) Pin=Y Related=A combinational fall_transition ...
Sep 26 16:36:12 Thread 0: Cell=NOR2X1 (83%) Pin=Y Related=B combinational fall_transition ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (87%) Pin=A Related= rising_edge rise_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (91%) Pin=A Related= falling_edge fall_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (95%) Pin=B Related= rising_edge rise_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (100%) Pin=B Related= falling_edge fall_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (100%) Pin= Related= combinational leakage_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (100%) Pin= Related= combinational leakage_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (100%) Pin= Related= combinational leakage_power ...
Sep 26 16:36:13 Thread 0: Cell=NOR2X1 (100%) Pin= Related= combinational leakage_power ...
Performance statistics for NOR2X1: Spectre cpu time = 0.8 seconds, total cpu time = 0.9 seconds, wall clock time = 1.0 seconds.

Characterizing INVX1 (3)
Sep 26 16:36:13 Thread 0: Cell=INVX1 (50%) Pin=Y Related=A combinational rise_transition ...
Sep 26 16:36:13 Thread 0: Cell=INVX1 (100%) Pin=Y Related=A combinational fall_transition ...
Sep 26 16:36:13 Thread 0: Cell=INVX1 (100%) Pin= Related= combinational leakage_power ...
Sep 26 16:36:13 Thread 0: Cell=INVX1 (100%) Pin= Related= combinational leakage_power ...
Performance statistics for INVX1: Spectre cpu time = 0.3 seconds, total cpu time = 0.3 seconds, wall clock time = 0.0 seconds.
```

```
INFO: Write Liberty
LIBERATE parameter "mx_format_expand_buses" set to "0"
LIBERATE parameter "ecsm_multi_stage_cap_mode" set to "0"
LIBERATE parameter "ccsp_mode" set to "0"
LIBERATE parameter "enable_command_history" set to "0"
WARNING (LIB-5015): (write_library): The existing library file '/home/elb/VLSI/Liberate-test/libtest/lib/Lib6710_XX.lib' was renamed to '/home/elb/VLSI/Liberate-test/libtest/lib/Lib6710_XX.lib.5'.
Writing library to /home/elb/VLSI/Liberate-test/libtest/lib/Lib6710_XX.lib, started at Tue Sep 26 16:36:14 MDT 2017
Writing .lib for cell INVX1
LIBERATE parameter "sdf_cond_warning" set to "0"
Writing .lib for cell NAND2X1
Writing .lib for cell NOR2X1
Writing .lib for cell TIEHI
Writing .lib for cell TIELO
LIBERATE parameter "ccsp_table_reduction" set to "1"
Number of passing cells = 5
Number of failing cells = 0
List of failing cells {}
Finished writing 5 cells to library /home/elb/VLSI/Liberate-test/libtest/lib/Lib6710_XX.lib at Tue Sep 26 16:36:15 MDT 2017
LIBERATE parameter "write_sens_nchange" set to "1"
Peak memory usage: 413 MB
Peak virtual memory usage: 360 MB
Peak physical memory usage: 54 MB
Wall time : 0.00 hours (17.00 seconds)
LIBERATE exited on lab2-20.eng.utah.edu at Tue Sep 26 16:36:15 MDT 2017

[elb@lab2-20 libtest]$
```

Changing library name in .lib

```
emac25.2@lab2-20.eng.utah.edu
File Edit Options Buffers Tools Help
Library (Lib6710_XX) {
/* Models written by Liberate 16.1.3.111 from Cadence Design Systems, Inc. on Sun Sep 24 18:57:32 MDT 2017 */
comment : "";
date : "$Date: Sun Sep 24 18:56:55 2017 $";
revision : "1.0";
delay_model : table_lookup;
capacitive_load_unit (1,pf);
current_unit : "1mA";
leakage_power_unit : "1nW";
pulling_resistance_unit : "1kohm";
time_unit : "1ns";
voltage_unit : "1V";
voltage_map (vdd, 5);
voltage_map (vss, 0);
default_cell_leakage_power : 0;
default_fanout_load : 1;
default_max_transition : 1.2;
default_output_pin_cap : 0;
in_place_swap_mode : match_footprint;
input_threshold_pct_fall : 70;
input_threshold_pct_rise : 30;
nom_process : 1;
nom_temperature : 25;
nom_voltage : 5;
output_threshold_pct_fall : 30;
output_threshold_pct_rise : 70;
slow_derate_from_library : 1;
slow_lower_threshold_pct_fall : 20;
slow_lower_threshold_pct_rise : 20;
slow_upper_threshold_pct_fall : 80;
slow_upper_threshold_pct_rise : 80;
operating_conditions (PVT_5V_25C) {
process : 1;
temperature : 25;
voltage : 5;
}
}

--:--- Lib6710_XX.lib Top L1 (Fundamental)
```

```

emacs-25.2@lab2-20.eng.utah.edu
File Edit Options Buffers Tools Help

cell (INVX1) {
  area : 129.6;
  cell_footprint : "INV";
  cell_leakage_power : 0.0500074;
  pg_pin (vdd) {
    pg_type : primary_power;
    voltage_name : "vdd";
  }
  pg_pin (vss) {
    pg_type : primary_ground;
    voltage_name : "vss";
  }
  leakage_power () {
    value : 0.0500012;
    when : "(A * !Y)";
    related_pg_pin : vdd;
  }
  leakage_power () {
    value : 0.05000137;
    when : "(!A * Y)";
    related_pg_pin : vdd;
  }
  leakage_power () {
    value : 0.0500074;
    related_pg_pin : vdd;
  }
  pin (Y) {
    direction : output;
    function : "!A";
    min_capacitance : 0.01;
    power_down_function : "(!vdd) + (vss)";
    related_ground_pin : vss;
  }
}
--:--- CAD06.lib 52% L5242 (Fundamental)

```

```

emacs-25.2@lab2-20.eng.utah.edu
File Edit Options Buffers Tools Help

pin (Y) {
  direction : output;
  function : "!A";
  min_capacitance : 0.01;
  power_down_function : "(!vdd) + (vss)";
  related_ground_pin : vss;
  related_power_pin : vdd;
  max_capacitance : 0.6;
  timing () {
    related_pin : "A";
    timing_sense : negative_unate;
    timing_type : combinational;
    cell_rise (delay_template_5x5_X1) {
      index_1 ("0.06, 0.18, 0.42, 0.6, 1.2");
      index_2 ("0.01, 0.05, 0.1, 0.3, 0.6");
      values ( \
        "0.112696, 0.224034, 0.362374, 0.914454, 1.74143", \
        "0.184577, 0.301391, 0.43794, 0.98744, 1.81386", \
        "0.304229, 0.450398, 0.59735, 1.14043, 1.96319", \
        "0.385552, 0.549684, 0.710877, 1.25817, 2.0774", \
        "0.634888, 0.847663, 1.04606, 1.65921, 2.46975" \
      );
    }
    rise_transition (delay_template_5x5_X1) {
      index_1 ("0.06, 0.18, 0.42, 0.6, 1.2");
      index_2 ("0.01, 0.05, 0.1, 0.3, 0.6");
      values ( \
        "0.0657055, 0.169969, 0.304816, 0.844863, 1.65462", \
        "0.0971017, 0.186204, 0.309307, 0.844673, 1.65416", \
        "0.148417, 0.248856, 0.35929, 0.850247, 1.65428", \
        "0.182127, 0.291049, 0.408904, 0.872642, 1.65491", \
        "0.277852, 0.421202, 0.552645, 1.00554, 1.71487" \
      );
    }
  }
}
--:--- CAD06.lib 52% L5284 (Fundamental)

```

Converting .lib to .db

```
[elb@lab2-20 lib]$ syn-lc
Using setup-synopsys from S17
Assuming your OS is amd64
You are now set up to run the synopsys tools.

Working directory is /home/elb/VLSI/Liberate/lib

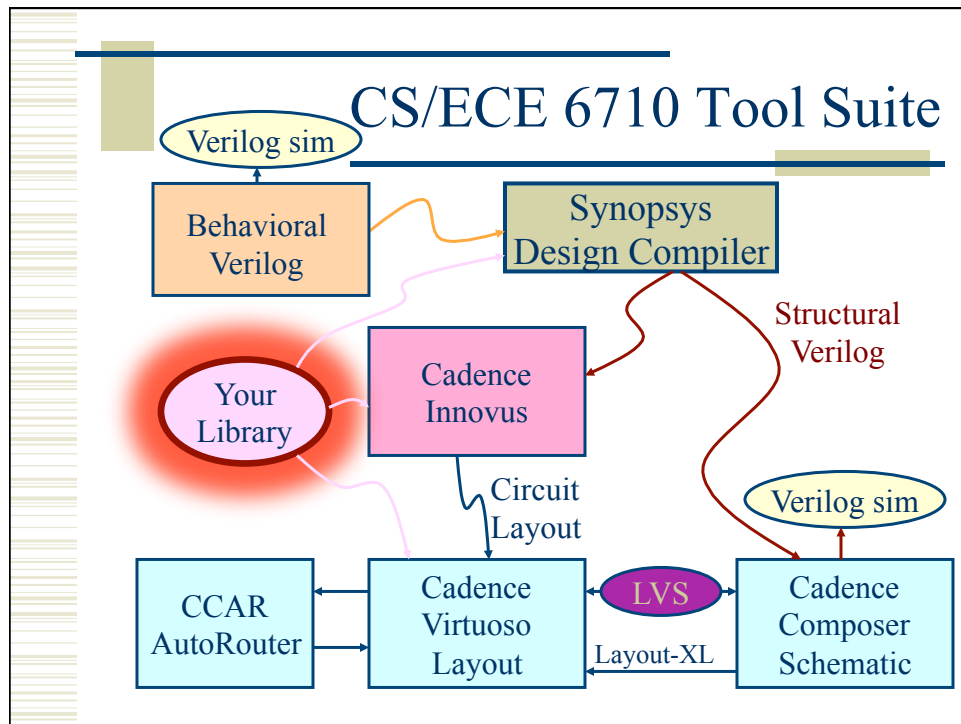
-----
Library Compiler (TM)
DesignWare (R)
Version M-2016.12-SP3 for linux64 - Apr 13, 2017
Copyright (c) 1988 - 2017 Synopsys, Inc.
This software and the associated documentation are proprietary to Synopsys, Inc.
This software may only be used in accordance with the terms and conditions
of a written license agreement with Synopsys, Inc. All other use, reproduction,
or distribution of this software is strictly prohibited.
-----

Initializing...
lc_shell> read_lib Lib6710_XX.lib
Reading '/home/elb/VLSI/Liberate/lib/Lib6710_XX.lib' ...
Warning: Line 1, The 'default_inout_pin_cap' attribute is not specified. Using 1.00. (LBDB-172)
Warning: Line 1, The 'default_input_pin_cap' attribute is not specified. Using 1.00. (LBDB-172)
Warning: Line 1, The 'default_leakage_power_density' attribute is not specified. Using 0.00. (LBDB-172)
Warning: Line 105, Cell 'INVX1', The cell leakage power attribute of the 'INVX1' cell is redundant
and not used in the leakage power modeling. (LBDB-644)
Warning: Line 215, Cell 'INVX1', pin 'A', The pin 'A' does not have a internal_power group. (LBDB-607)
Warning: Line 229, Cell 'NAND2X1', The cell leakage power attribute of the 'NAND2X1' cell is redundant
and not used in the leakage power modeling. (LBDB-644) Technology library
'Lib6710_XX' read successfully
1
```

Converting .lib to .db

```
lc_shell> write_lib Lib6710_XX -o Lib6710_XX.db Wrote the
'Lib6710_XX' library to '/home/elb/VLSI/Liberate/lib/Lib6710_XX.db' successfully
1
lc_shell> exit Memory usage for this session 19 Mbytes.
CPU usage for this session 0 seconds ( 0.00 hours ).

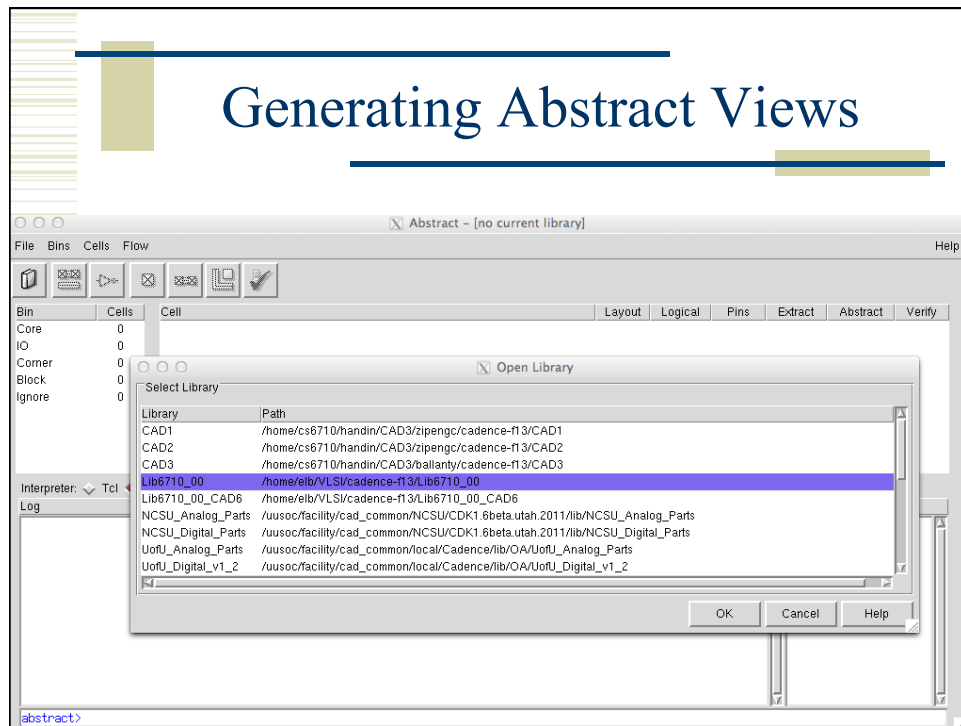
Thank you...
[elb@lab2-20 lib]$
```



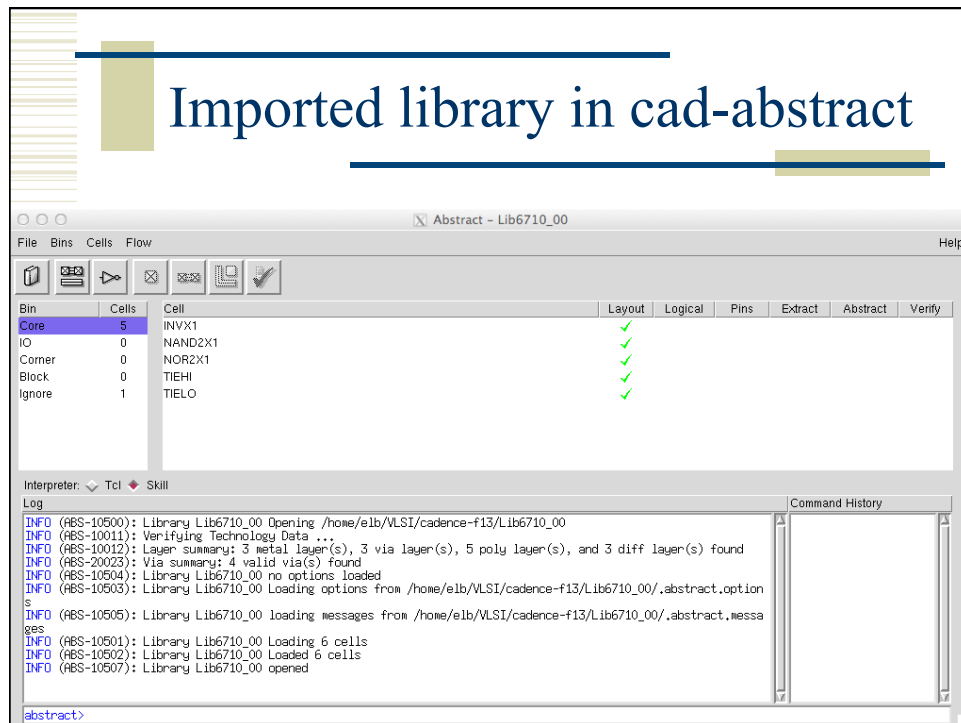
In the CAD Book

- ♦ Chapter 10 – Abstract Generation
 - Abstract views are used by place and route
 - Eventually they are captured in a .lef file that describes the place and route geometry

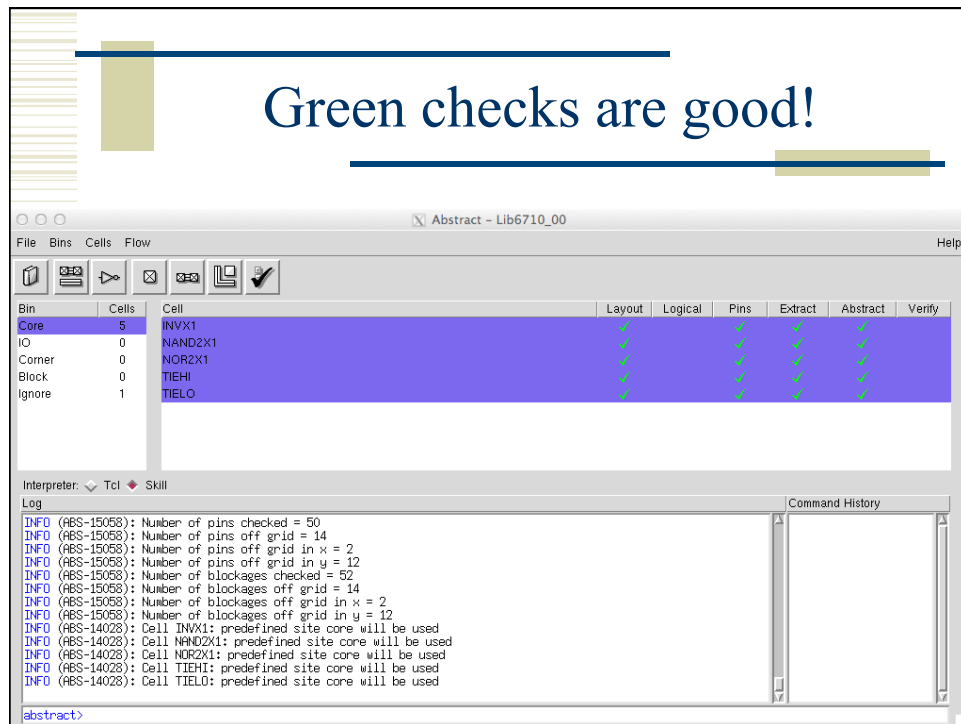
Generating Abstract Views



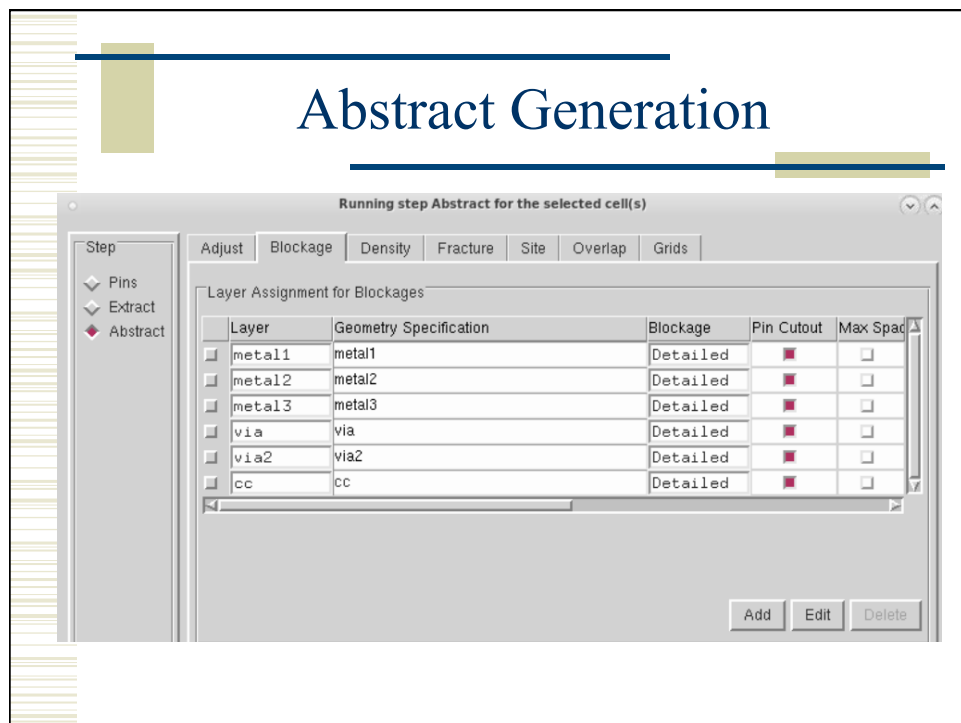
Imported library in cad-abstract



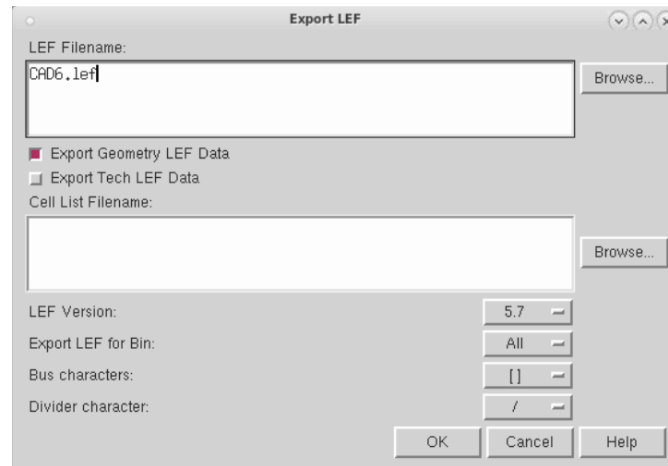
Green checks are good!



Abstract Generation



Export Lib6710_00.lef file



“geometry lef”

```
emacslab2-12.eng.utah.edu
File Edit Options Buffers Tools Help
VERSION 5.6 ;
BUSBITCHARS "[ ]" ;
DIVIDERCHAR "/" ;

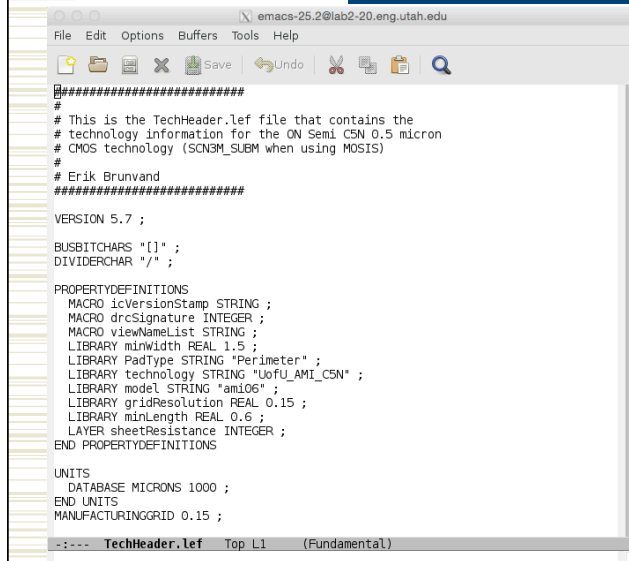
PROPERTYDEFINITIONS
  MACRO icVersionStamp STRING ;
  MACRO drcSignature INTEGER ;
END PROPERTYDEFINITIONS

MACRO INVX1
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN INVX1 0 0 ;
  SIZE 4.8 BY 27 ;
  SYMMETRY X Y ;
  SITE core ;
  PIN gnd!
  DIRECTION INOUT ;
  USE GROUND ;
  SHAPE ABUTMENT ;
  PORT
    LAYER metall ;
    RECT 0.6 -1.2 1.8 3.15 ;
    RECT -1.2 -1.2 6 1.2 ;
  END
END gnd!
PIN vdd!
DIRECTION INOUT ;
USE POWER ;

Lib6710_00.lef Top L9 (Fundamental)
```

Replace highlighted
text with
TechHeader.lef
from Liberate
directory

“technology lef”



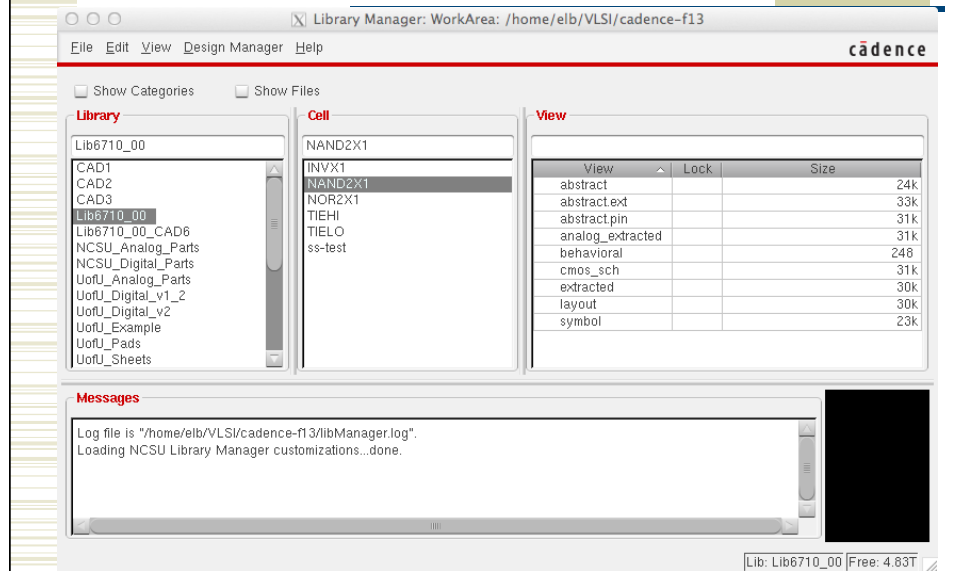
```
*****
#
# This is the TechHeader.lef file that contains the
# technology information for the ON Semi C5N 0.5 micron
# CMOS technology (SCNM_SUBM when using MOSIS)
#
# Erik Brunvand
*****
VERSION 5.7 ;
BUSBITCHARS "[]* ;
DIVIDERCHAR "/" ;
PROPERTYDEFINITIONS
  MACRO icVersionStamp STRING ;
  MACRO drcSignature INTEGER ;
  MACRO viewNameList STRING ;
  LIBRARY minwidth REAL 1.5 ;
  LIBRARY PadType STRING "Perimeter" ;
  LIBRARY technology STRING "UoFU_AMI_C5N" ;
  LIBRARY model STRING "am106" ;
  LIBRARY gridResolution REAL 0.15 ;
  LIBRARY minLength REAL 0.6 ;
  LAYER sheetResistance INTEGER ;
END PROPERTYDEFINITIONS
UNITS
  DATABASE MICRONS 1000 ;
END UNITS
MANUFACTURINGGRID 0.15 ;
```

Replace highlighted
text with
TechHeader.lef
from class
directory

Final CAD5 Files...

- ◆ *Nine views of every cell*
 - abstract, abstract.ext, abstract.pin, analog_extracted, behavioral, cmos_sch, extracted, layout, symbol
 - DRC and LVS-checked, and simulated
- ◆ *Three versions of the library description*
 - Lib6710_00.lib // timing information
 - Lib6710_00.db // design compiler target lib
 - Lib6710_00.lef // place and route info

All Nine Views...



Test with beh2str

- `beh2str addsub.v addsub_dc.v Lib6710_00.db`
- ◆ **Results in addsub_dc.v and addsub_dc.v.rep**
- ◆ *NOTE! Your 5-cell library has no DFF, so you can't synthesize any sequential circuits!*
 - *Combinational circuits only at this point...*

addsub_dc.v

```
module addsub ( a, b, addnsub, result );
  input [7:0] a;
  input [7:0] b;
  output [8:0] result;
  input addnsub;
  wire  n26, n27, n28, n29, n30, n31, n32, n33, n34, n35, n36, n37, n38, n39,
        n40, n41, n42, n43, n44, n45, n46, n47, n48, n49, n50, n51, n52, n53,
        n54, n55, n56, n57, n58, n59, n60, n61, n62, n63, n64, n65, n66, n67,
  ...

  NAND2X1 U33 ( .A(n26), .B(n27), .Y(result[8]) );
  NAND2X1 U34 ( .A(b[7]), .B(n28), .Y(n27) );
  NAND2X1 U35 ( .A(n29), .B(n30), .Y(n28) );
  NOR2X1 U36 ( .A(n31), .B(n32), .Y(n29) );
  ...
  NOR2X1 U216 ( .A(n188), .B(a[0]), .Y(n175) );
  NAND2X1 U217 ( .A(a[0]), .B(n188), .Y(n202) );
  INVX1 U218 ( .A(b[0]), .Y(n188) );
endmodule
```

addsub_dc.v.rep

Operating Conditions: typical Library: Lib6710_00

Wire Load Model Mode: top

Startpoint: b[1] (input port)

Endpoint: result[8] (output port)

Path Group: (none)

Path Type: max

Point	Incr	Path

input external delay	0.00	0.00 r
b[1] (in)	0.00	0.00 r
U198/Y (NOR2X1)	0.50	0.50 f
U194/Y (NOR2X1)	0.36	0.86 r
...		
U34/Y (NAND2X1)	0.25	10.16 f
U33/Y (NAND2X1)	0.24	10.40 r
result[8] (out)	0.00	10.40 r
data arrival time		10.40

(Path is unconstrained)

addsub_dc.v.rep

Library(s) Used:

Lib6710_00 (File: /home/elb/VLSI/cadence-f13/syn-f13/CAD5test/
Lib6710_00.db)

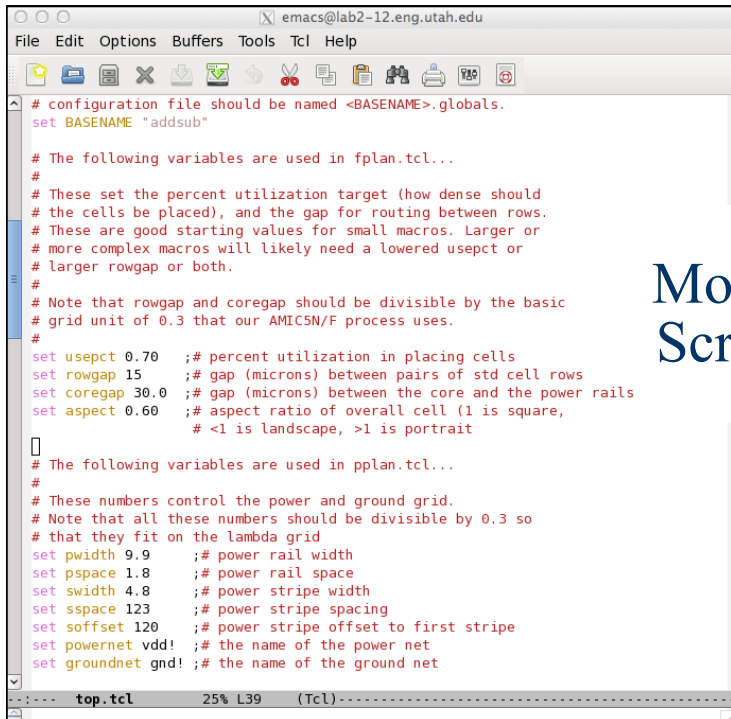
Number of ports:	26
Number of nets:	203
Number of cells:	186
Number of combinational cells:	186
Number of sequential cells:	0
Number of macros:	0
Number of buf/inv:	37
Number of references:	3

Summary

- ◆ You now have a library that is fully functional
 - BUT – only on combinational circuits
 - No DFF yet!
- ◆ Every step of the way requires extreme care to get things exactly right
 - No trick to finding the right answer
 - The point is to practice working with the data & tools

Look ahead to Innovus

```
[elb@lab2-12 addsub]$ ll -t
total 132
-rw-r--r-- 1 elb cs-rsrch 1522 Oct 10 2013 addsub.globals
-rw-r--r-- 1 elb cs-rsrch 3814 Oct 10 2013 top.tcl
-rw-r--r-- 1 elb cs-rsrch 2618 Oct 10 2013 mmnc.tcl
-rw-r--r-- 1 elb cs-rsrch 288 Oct 10 16:39 Lib6710_00.v
-rw-r--r-- 1 elb cs-rsrch 22736 Oct 10 16:39 Lib6710_00.lib
-rw-r--r-- 1 elb cs-rsrch 31744 Oct 10 16:39 Lib6710_00.db
-rw-r--r-- 1 elb cs-rsrch 11919 Oct 10 16:39 Lib6710_00.lef
-rw-r--r-- 1 elb cs-rsrch 3413 Oct 10 16:39 addsub_struct.sdc
-rw-r--r-- 1 elb cs-rsrch 11742 Oct 10 16:39 addsub_struct.v
-rw-r--r-- 1 elb cs-rsrch 2016 Oct 10 16:37 verify.tcl
-rw-r--r-- 1 elb cs-rsrch 3005 Oct 10 16:37 route.tcl
-rw-r--r-- 1 elb cs-rsrch 2394 Oct 10 16:37 pplan.tcl
-rw-r--r-- 1 elb cs-rsrch 1940 Oct 10 16:37 place.tcl
-rw-r--r-- 1 elb cs-rsrch 971 Oct 10 16:37 fplan.tcl
-rw-r--r-- 1 elb cs-rsrch 1641 Oct 10 16:37 cts.tcl
[elb@lab2-12 addsub]$
```



```
# configuration file should be named <BASENAME>.globals.
set BASENAME "addsub"

#
# The following variables are used in fplan.tcl...
#
# These set the percent utilization target (how dense should
# the cells be placed), and the gap for routing between rows.
# These are good starting values for small macros. Larger or
# more complex macros will likely need a lowered usepct or
# larger rowgap or both.
#
# Note that rowgap and coregap should be divisible by the basic
# grid unit of 0.3 that our AMIC5N/F process uses.
#
set usepct 0.70 ;# percent utilization in placing cells
set rowgap 15 ;# gap (microns) between pairs of std cell rows
set coregap 30.0 ;# gap (microns) between the core and the power rails
set aspect 0.60 ;# aspect ratio of overall cell (1 is square,
                ;# <1 is landscape, >1 is portrait)

#
# The following variables are used in pplan.tcl...
#
# These numbers control the power and ground grid.
# Note that all these numbers should be divisible by 0.3 so
# that they fit on the lambda grid
set pwidth 9.9 ;# power rail width
set pspace 1.8 ;# power rail space
set swidth 4.8 ;# power stripe width
set sspace 123 ;# power stripe spacing
set soffset 120 ;# power stripe offset to first stripe
set powernet vdd! ;# the name of the power net
set groundnet gnd! ;# the name of the ground net
```

Modify the Script Files

```
emacs@lab2-12.eng.utah.edu
File Edit Options Buffers Tools Help

#####
#
# Encounter Input configuration file
# University of Utah - 6710
#
# Use this file to describe the input files for
# placement and routing.
#
# This file is a ".globals" file for EDI 11
# and above.
#
# Look for terms surrounded by !!...!!
# These are the things you will need to change
#####
#
# Set the name of your structural Verlog file
# This comes from Synopsys synthesis
set init_verilog {addsub_struct.v}
# Set the name of your top module
set init_design {addsub}
# Set the name of your .lef file
# This comes from ELC
set init_lef_file {Lib6710_00.lef}

#####
# below here you probably don't have to change anything
#####
# Set the name of your "multi-mode-multi-corner data file
# You don't need to change this unless you're using a
# different mmmc.tcl file.
set init_mmmc_file {mmmc.tcl}
# Some helpful input mode settings
set init_import_mode {-treatUndefinedCellAsBbox 0 -keepEmptyModule 1}
# Set the names of your gnd and power nets
set init_gnd_net {gnd!}
set init_pwr_net {vdd!}

--... addsub.globals Top L31 (Fundamental)-----
Beginning of buffer
```

Modify the Script Files

```
emacs@lab2-12.eng.utah.edu
File Edit Options Buffers Tools Tcl Help

#####
#
# Encounter Multi-Mode Multi-Corner input file
# University of Utah - 6710
#
# This defines the timing libraries and RC
# extraction data to use. In EDI 11 and above
# all runs are specified as mmmc, even if you're
# only using one mode and one corner...
#
#####
# set the name of your .lib file
# You can create multiple library sets if you have multiple libraries
# such as fast, slow, and typ
# If you have multiple .lib files put them in a {list lib1 lib2} structure
create_library_set -name typical_lib \
-timing {Lib6710_00.lib}
# Specify the .sdc timing constraint file to use
create_constraint_mode -name typical_constraint \
-sdc_files {addsub_struct.sdc}
#
#####
# Below here you shouldn't have to change, unless you're doing
# something different than the basic EDI run...
#####
# Create an RC_corner that has specific capacitance info. If you have a
# "capTable," you can set it here (we don't have one yet for CSN) using:
# -cap_table capTable
# If you do have a capTable, you can do better optimization, including
# signal integrity optimization. These res and cap values are just defaults.
# They don't correspond to any particular process. You would have to do some
# digging to find more exact values for your process...
create_rc_corner -name typical_rc \
-preRoute_res {1.0} \

--... mmmc.tcl Top L1 (Tcl)-----
```

Modify the Script Files

