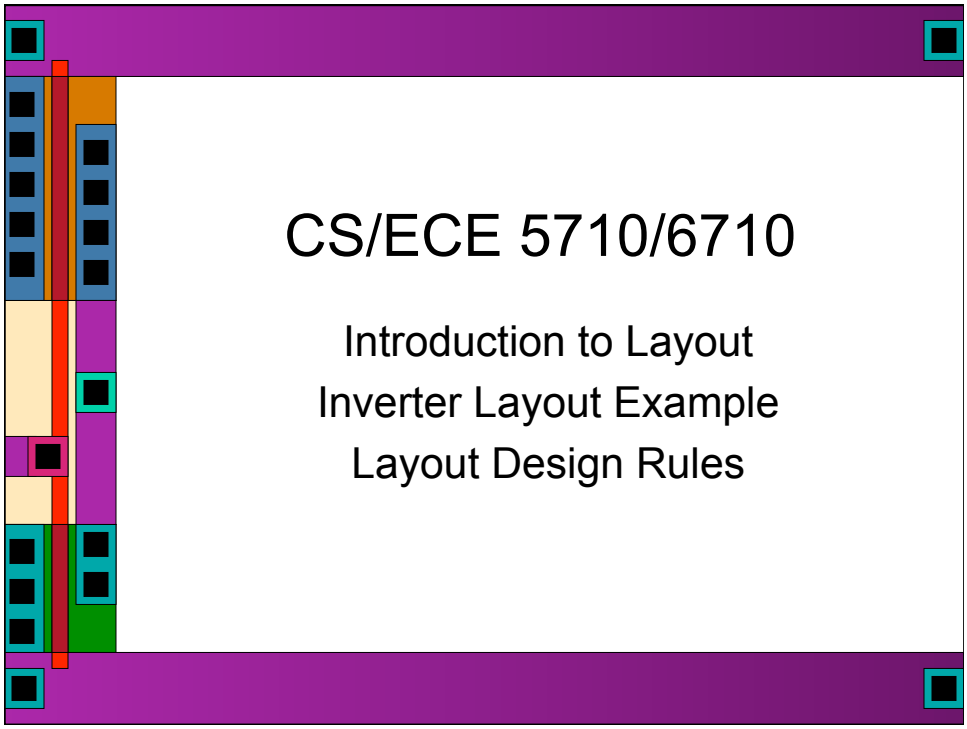
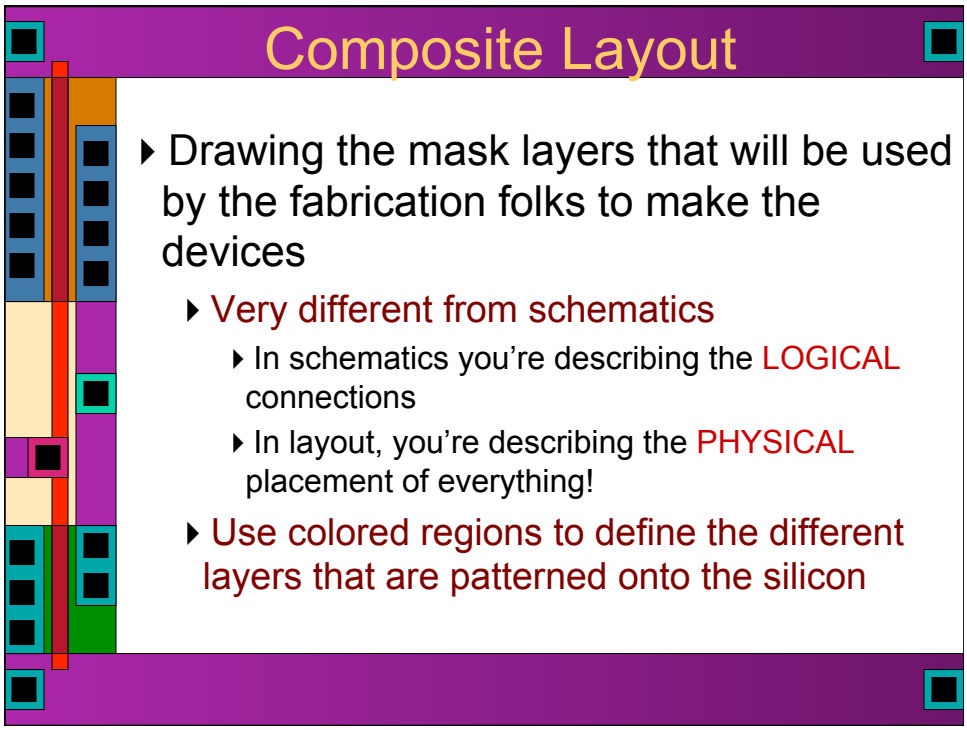


CS/ECE 5710/6710

Introduction to Layout

Inverter Layout Example

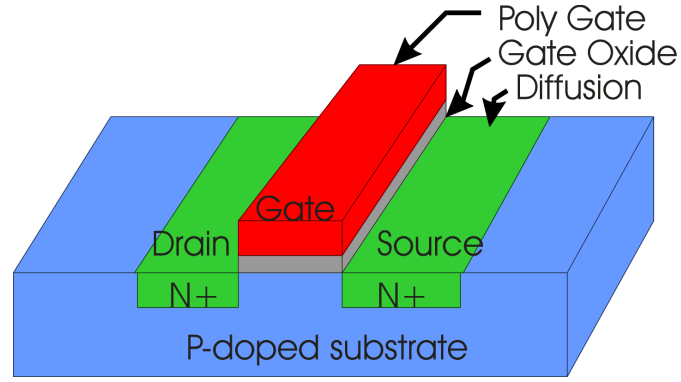
Layout Design Rules

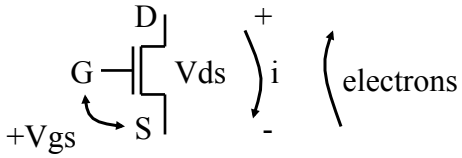


Composite Layout

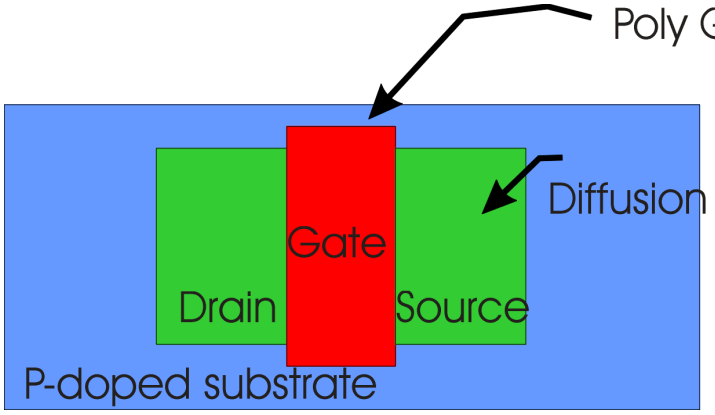
- Drawing the mask layers that will be used by the fabrication folks to make the devices
  - Very different from schematics
    - In schematics you're describing the LOGICAL connections
    - In layout, you're describing the PHYSICAL placement of everything!
  - Use colored regions to define the different layers that are patterned onto the silicon

N-type Transistor



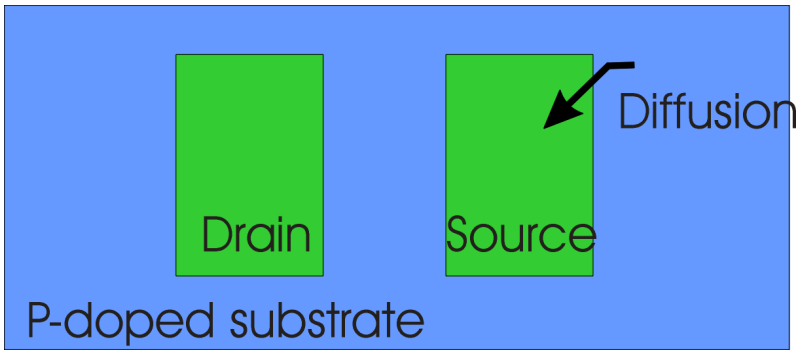


N-type from the top



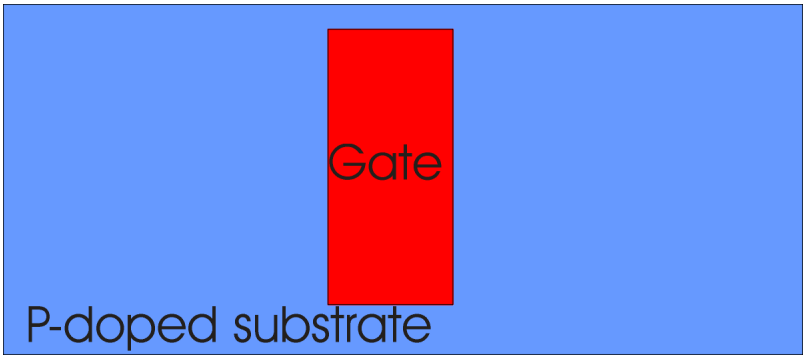
- Top view shows patterns that make up the transistor

Diffusion Mask



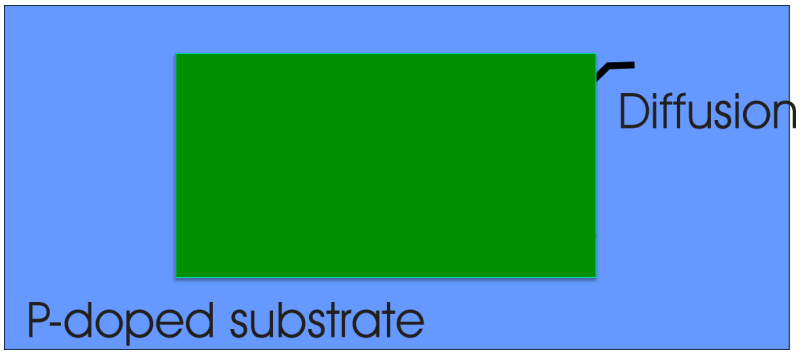
- Mask for just the diffused regions

Polysilicon Mask



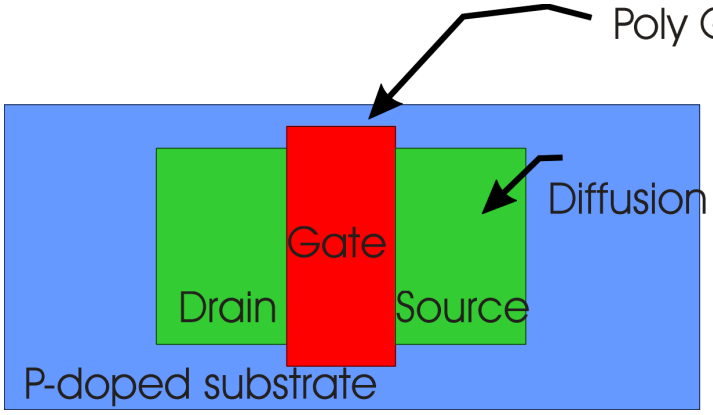
- Mask for just the polysilicon areas

Diffusion (active) Mask



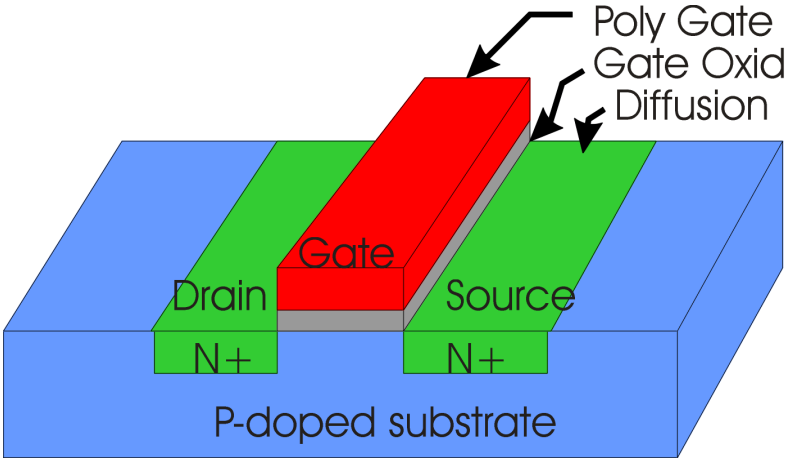
- Diffused (active) mask is actually drawn as a solid rectangle

Polysilicon Mask



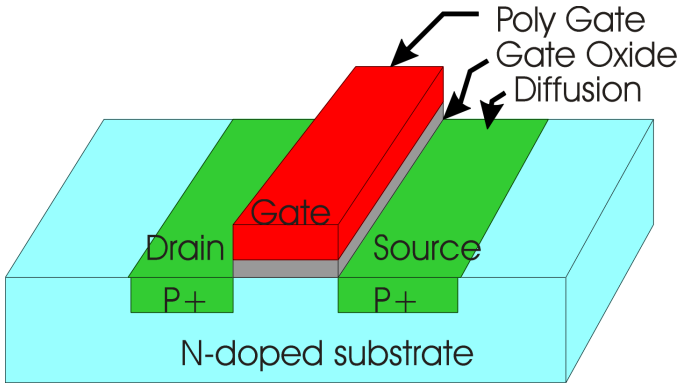
- Polysilicon mask goes on top of the active

Combine the two masks



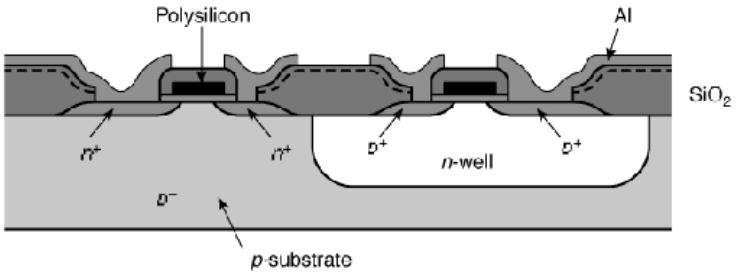
- You get an N-type transistor
  - There are other steps in the process…

P-type transistor



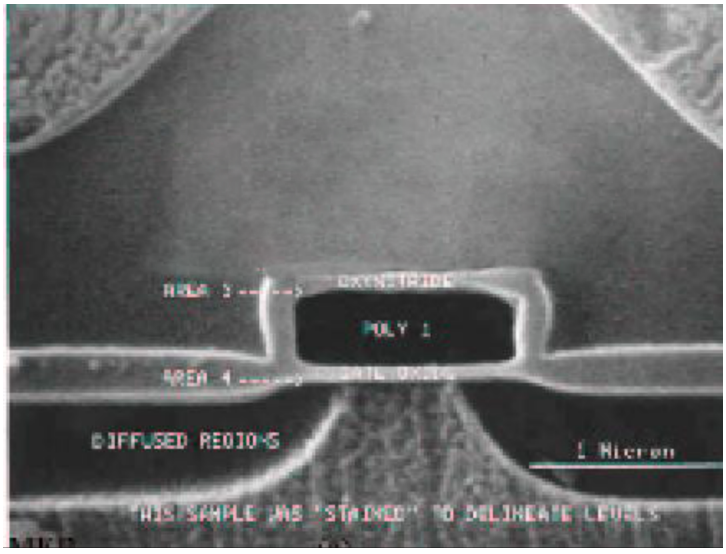
- Same type of masks as the N-type
  - But, you have to get the substrate right
  - and you have to dope the diffusion differently

General CMOS cross section



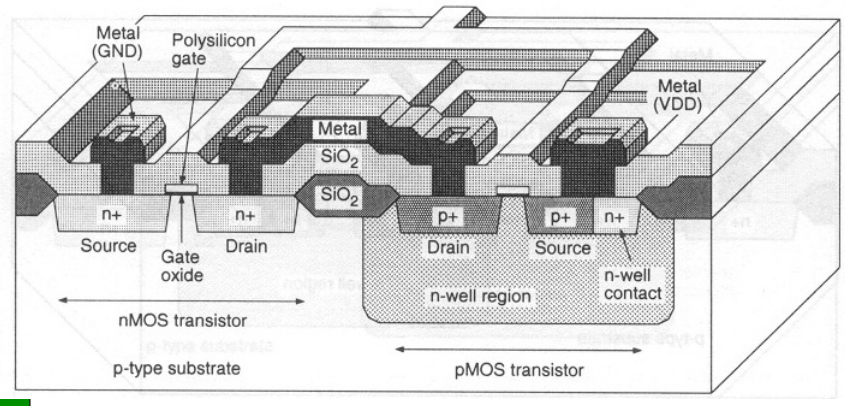
- Note that the general substrate is P-type
- The N-substrate for the P-transistor is in a “well”
- There are lots of other layers
  - Thick SiO_2 oxide (“field oxide”)
  - Thin SiO_2 oxide (“gate oxide”)
  - Metal for interconnect

Cutaway Photo

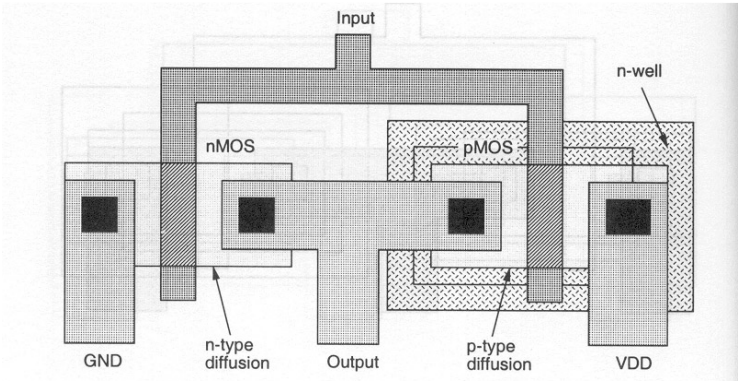


A Cutaway View

- CMOS structure with both transistor types, and top-view structure

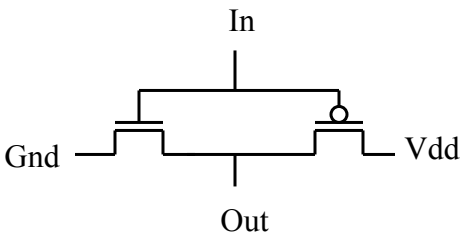


Top View from that Section

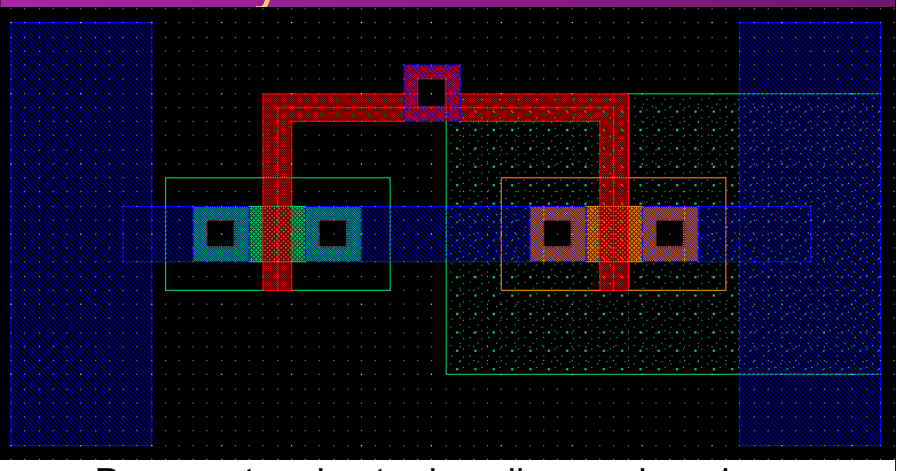


- Note the different mask layers that correspond to the different transistor layers
  - In particular, note the N-well and P-select layers

This is an Inverter

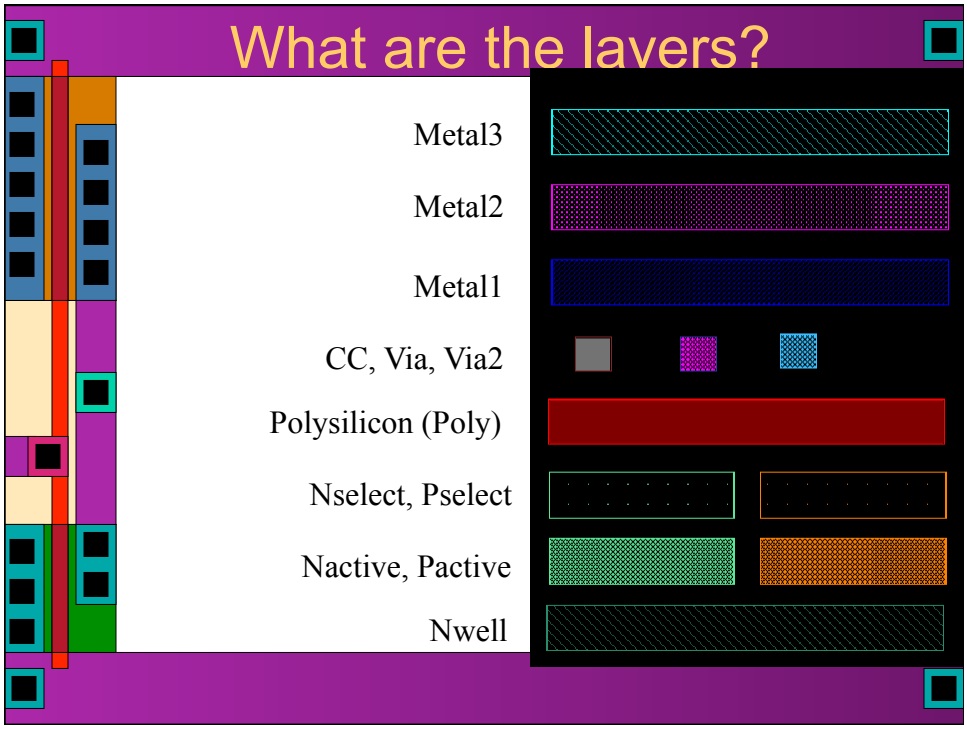


Layout in Cadence



- Draw rectangles to describe mask regions
- A LOT of things to keep in mind
  - connectivity, functionality, design rules

What are the lavers?



What are the layers?

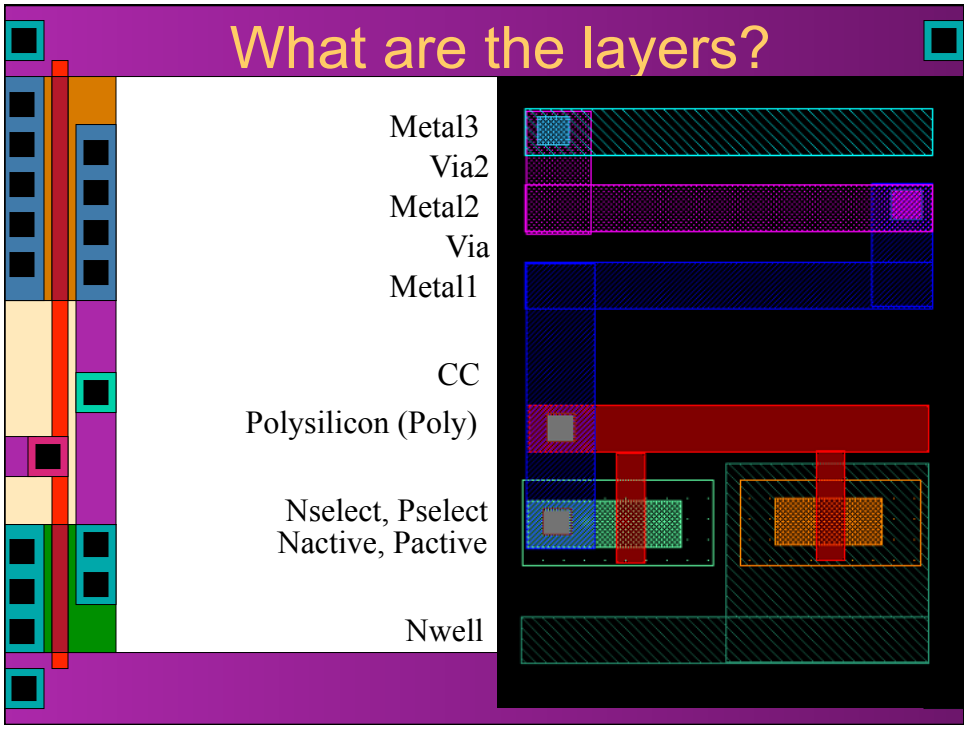
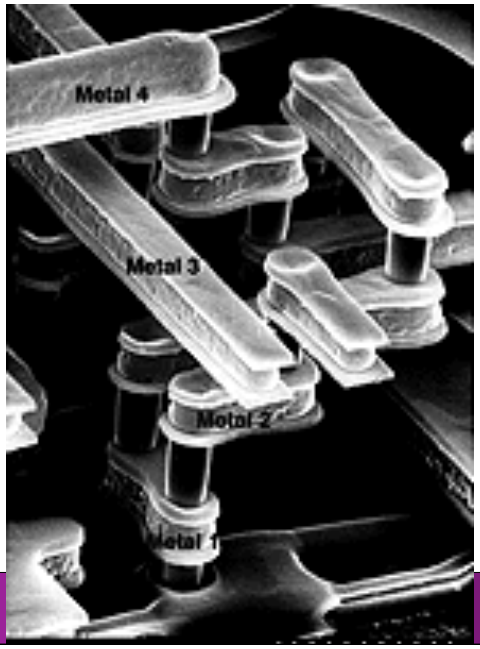
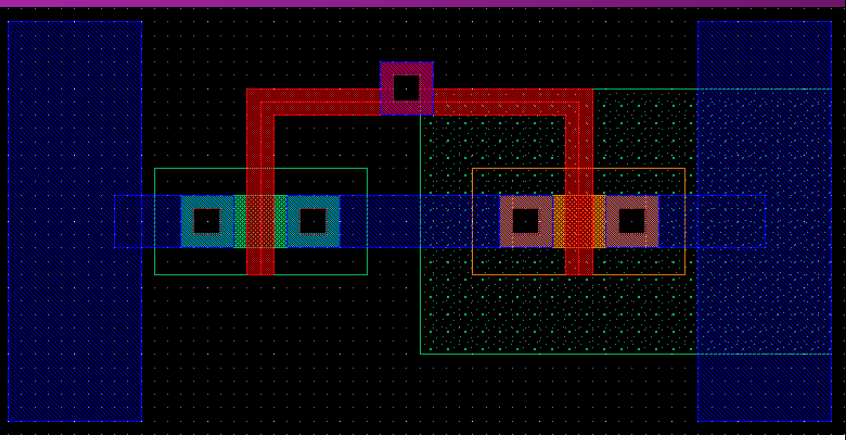


Photo of Interconnect

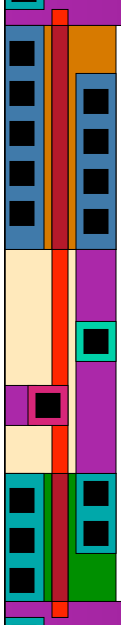


Back to the Inverter



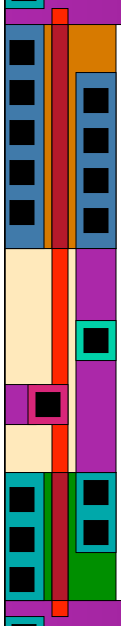
- Let's walk through drawing this inverter
- You can draw layers in whatever order makes sense to you…

Layout Basics



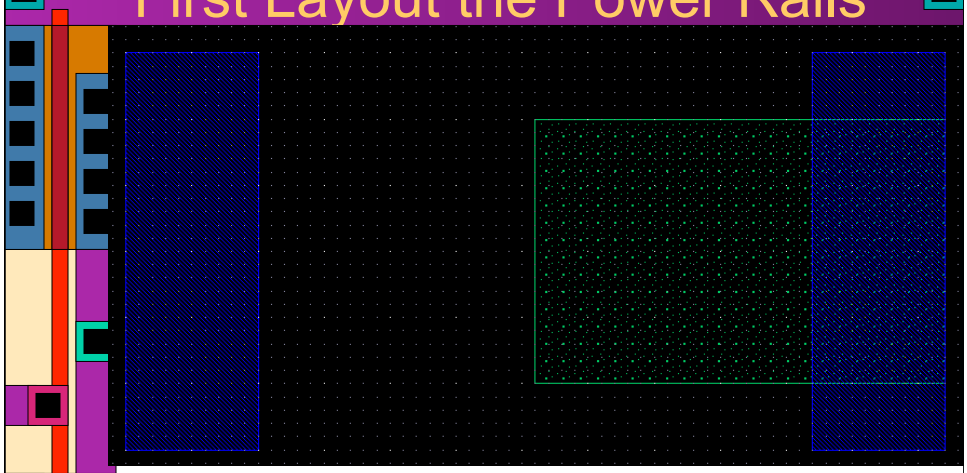
- Where poly crosses active = transistor
  - For N-type, nactive over the substrate (p substrate)
  - For P-type, pactive inside an Nwell
- There's really only one "active" mask
  - nselect and pselect layers define active types
  - Our setup has separate nactive and pactive colors to help keep things straight.

Layout Basics



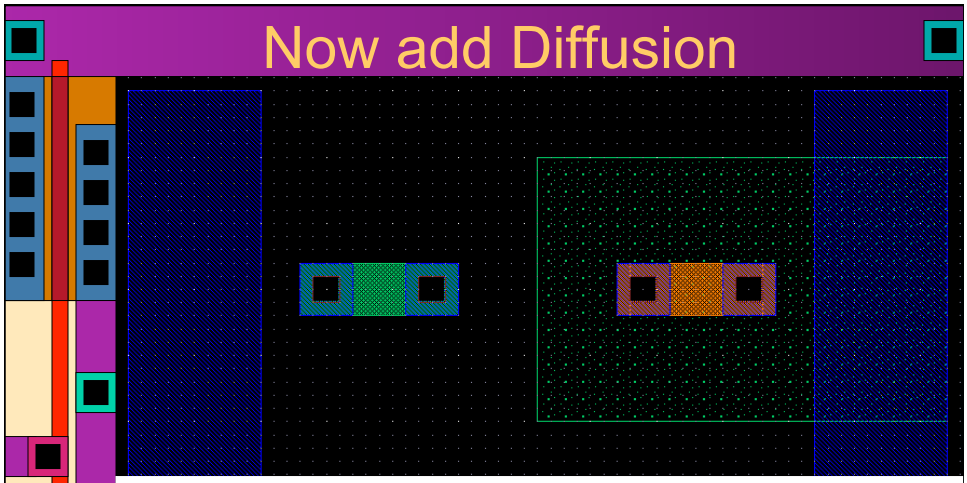
- Diffusion, Poly, and metal all conduct
  - But resistances are very different
    - Diffusion is worst, poly isn't too bad, metal is by far the best
- Contact cuts are needed to connect between layers
  - Make sure to use the right type of contact!
  - CC for poly-M1, nactive-M1, pactive-M1
  - Via1 for M1-M2
  - Via2 for M2-M3

First Layout the Power Rails



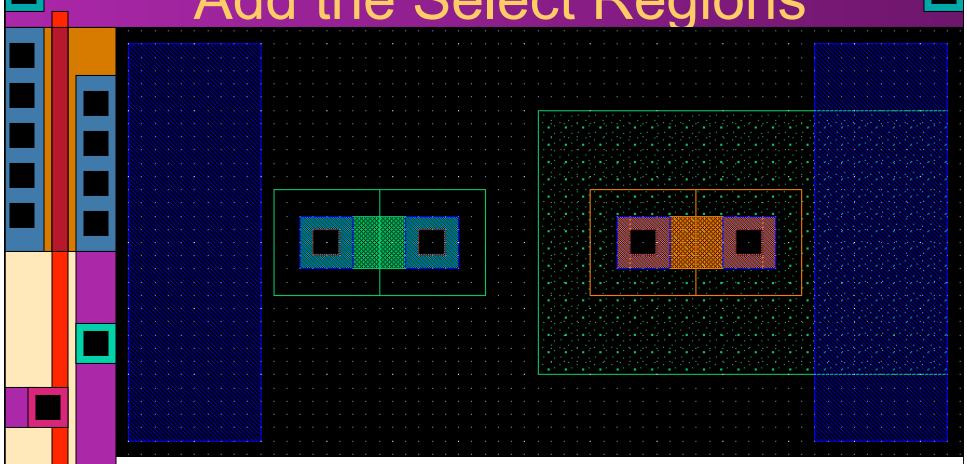
- Power rail pitch is important
  - Allows cells to connect by abutment
- Also add the N-well for the P-type transistor

Now add Diffusion



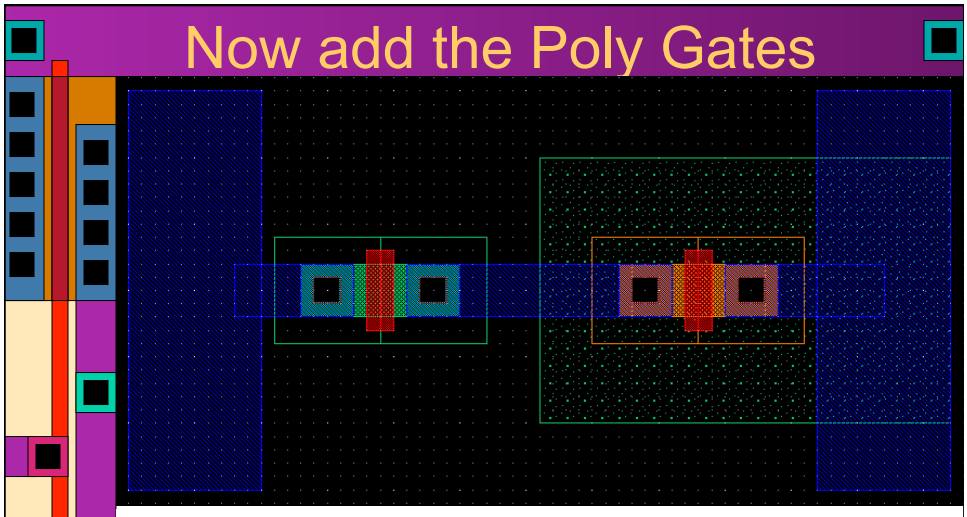
- Note the M1 contacts in the diffusion
- Diffusion by itself will be N-type
- Diffusion in an N-well will be P-type
  - Or will it? The well just defines the substrate type

Add the Select Regions



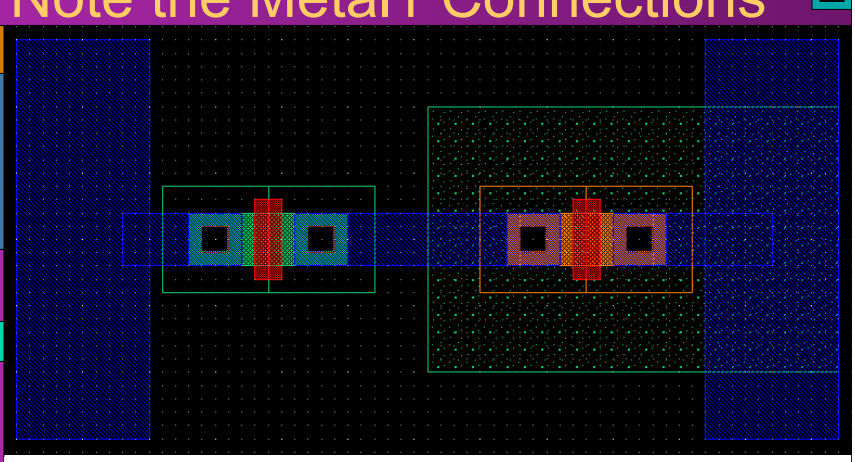
- Nselect defines N-type diffusion
- Pselect defines P-type diffusion

Now add the Poly Gates



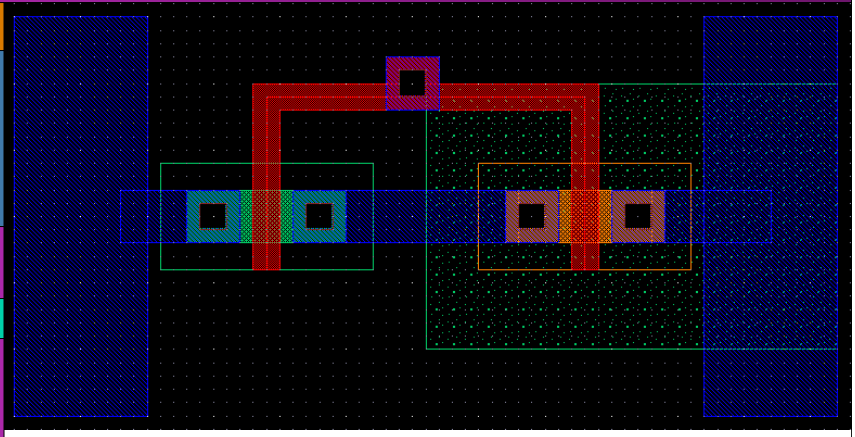
- Remember: crossing diffusion with Poly makes a transistor
  - The type of the diffusion, and the type of well, define what kind of transistor

Note the Metal1 Connections



- Overlapping boxes of the same type of material make a connection
- Overlaps of different types of material need a contact cut of some sort

Connect the Gates

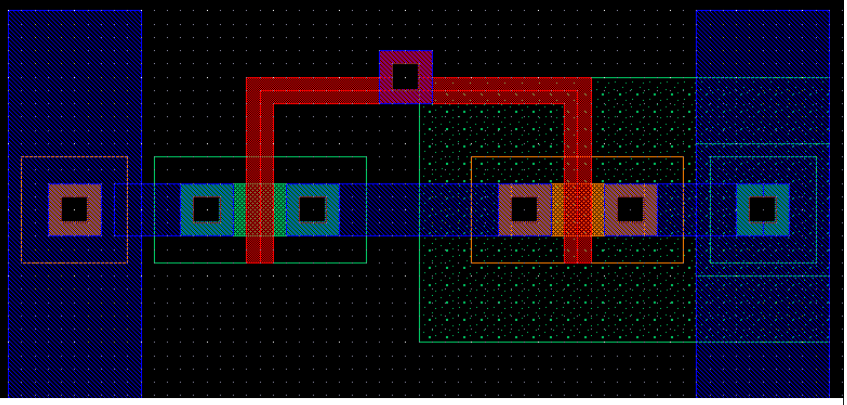


- Connect gates together to form the inverter
- Note contact cuts and metal overlaps

Layout Subtlety

- We currently think of transistors as three-terminal devices
  - Gate, Source, Drain
- They're really four-terminal devices
  - There's also a connection to the substrate
- It's important to tie the substrate to a specific voltage
  - GND for the P-substrate
  - VDD for the N-well
    - Make sure PN-diodes from active to substrate and well are reverse-biased…

Well (or Substrate) Contacts

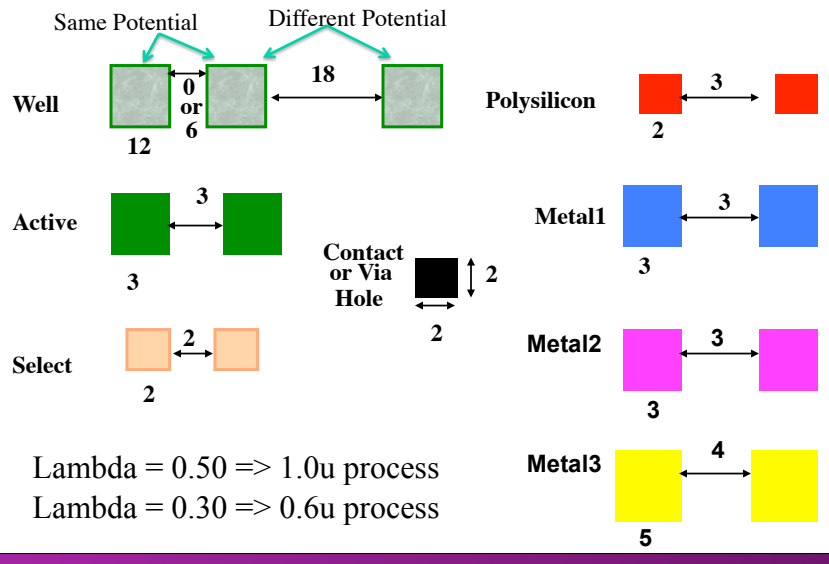


- Connect P-substrate to GND (VSS) with a little stub of P-type diffusion (remember pselect)
- Connect the N-well to VDD with a little stub of N-type diffusion
  - I.e. inside the N-well, but with nselect

Layout Design Rules

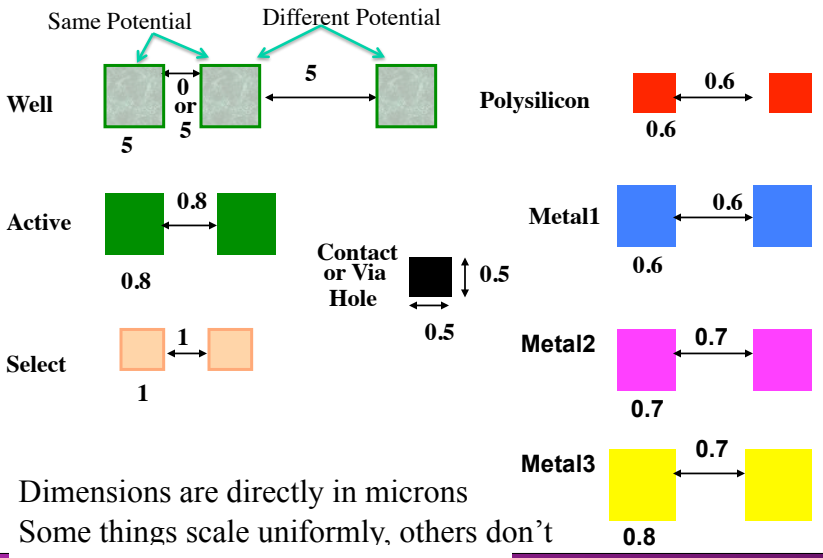
- Define the allowed geometry of the different layers
  - Guidelines for making safe process masks
  - Rules about the allowed sizes and shapes of a particular layer
  - Rules about how different layers interact
- Dimensions listed in one of two ways
  - Absolute dimensions (e.g. microns or nm)
  - Scalable dimensions in abstract units
    - Usually called “lambda”
    - Design in lambda units, then scale lambda for a particular process

Intra-Layer Rules (Lambda)



Lambda = 0.50 => 1.0u process
Lambda = 0.30 => 0.6u process

Intra-Layer Rules (Native)



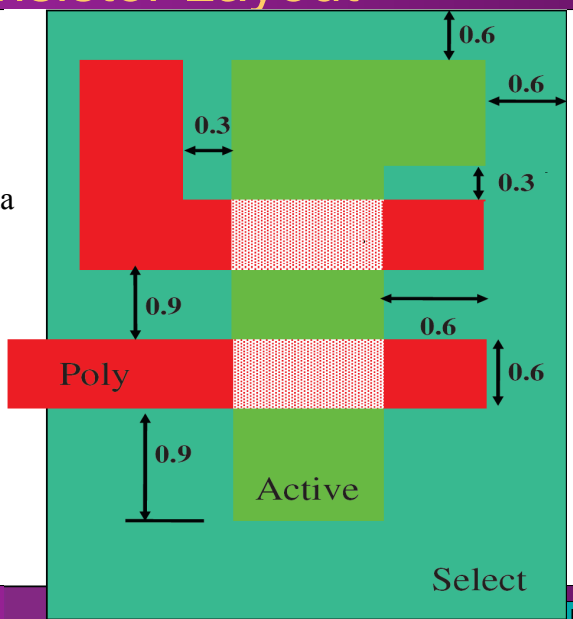
Dimensions are directly in microns

Some things scale uniformly, others don't

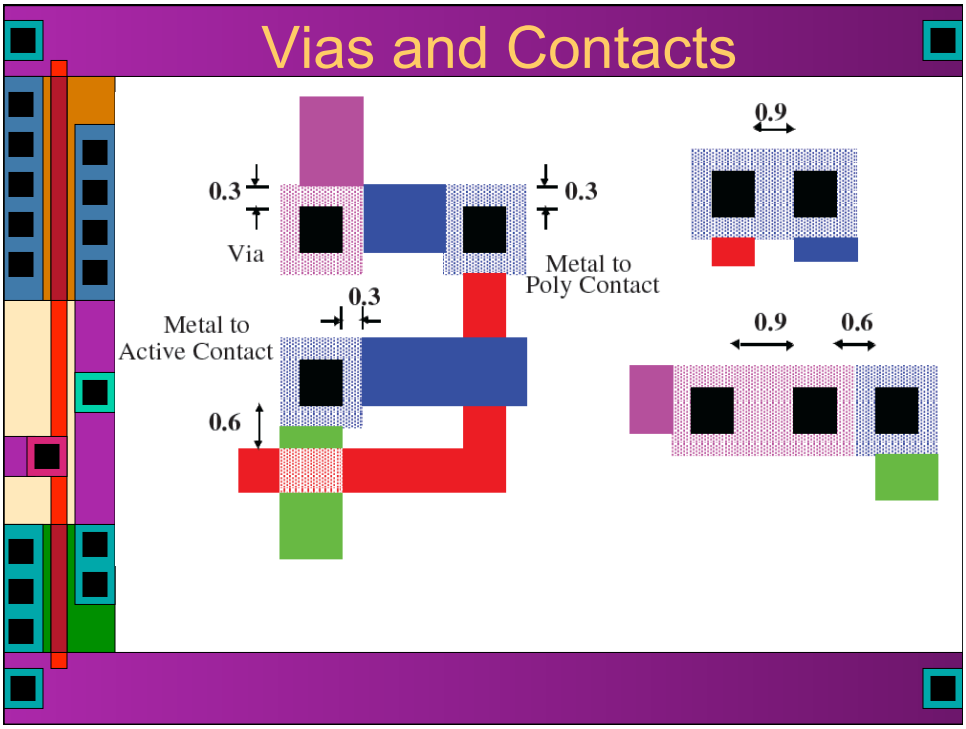
Native rules are generally more dense

Transistor Layout

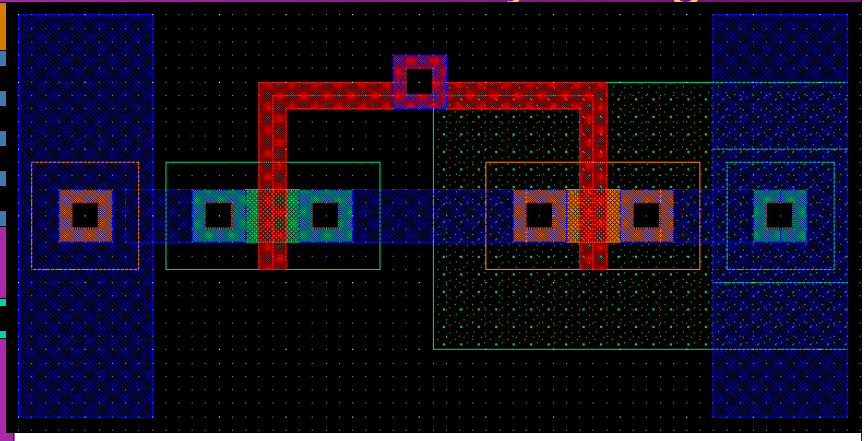
Measurements are in microns based on scalable rules and a lambda of 0.3.



Vias and Contacts



Look at Inverter Layout Again



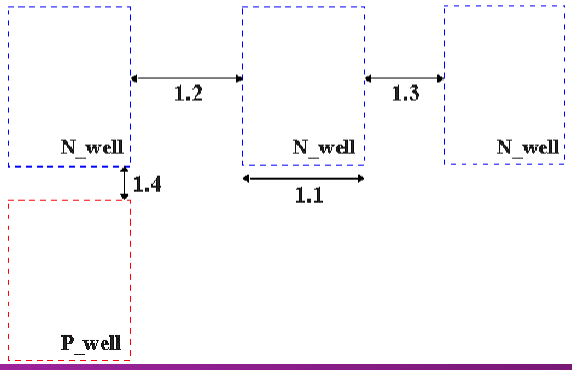
- Lots and lots of design rules to consider!
  - Use Design Rule Checking (DRC) to see if everything is OK

Layout Design Rules

- On the Canvas page
- Modified version of the MOSIS SCMOS Rev. 8 rules
  - Modified to show both Lambda and Micron dimensions
  - All our design will be done in microns
    - Because of the NCSU tech files
  - But, even though we're using microns, we're using the SCMOS Lambda rules…
- Print them out in color if possible!

SCMOS Nwell

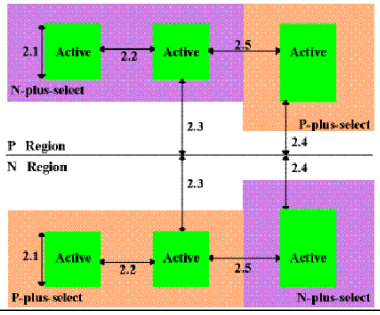
Rule	Description	SUBM	
		Lambda	Microns
1.1	Minimum width	12	3.6
1.2	Minimum spacing between wells at different potential	18	5.4
1.3	Minimum spacing between wells at same potential	6	1.8
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0



SCMOS Active (diffusion)

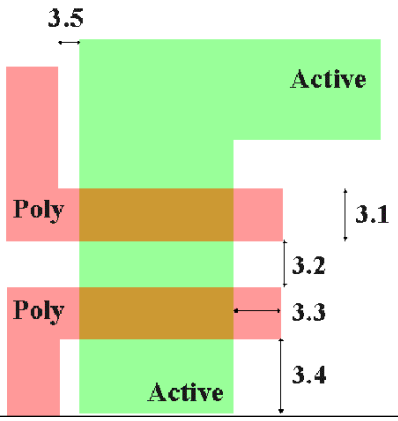
Rule	Description	SUBM	
		Lambda	Microns
2.1	Minimum width	3	0.9
2.2	Minimum spacing	3	0.9
2.3	Source/drain active to well edge	6	1.8
2.4	Substrate/well contact active to well edge	3	0.9
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	1.2

Note: For analog and critical digital designs, MOSIS recommends the minimum MOS *channel widths* (active under poly) to be 10 lambda i.e. 3 microns for submission to AMI ABN and C5N



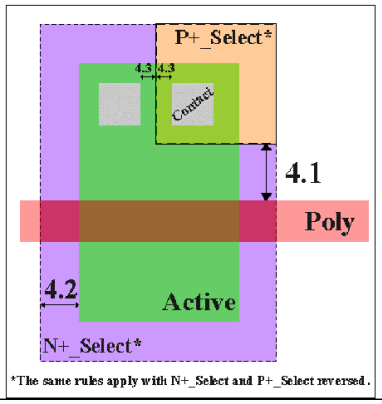
SCMOS Poly

Rule	Description	SUBM	
		Lambda	Microns
3.1	Minimum width	2	0.6
3.2	Minimum spacing over field	3	0.9
3.3	Minimum gate extension of active	2	0.6
3.4	Minimum active extension of poly	3	0.9
3.5	Minimum field poly to active	1	0.3



SCMOS Select

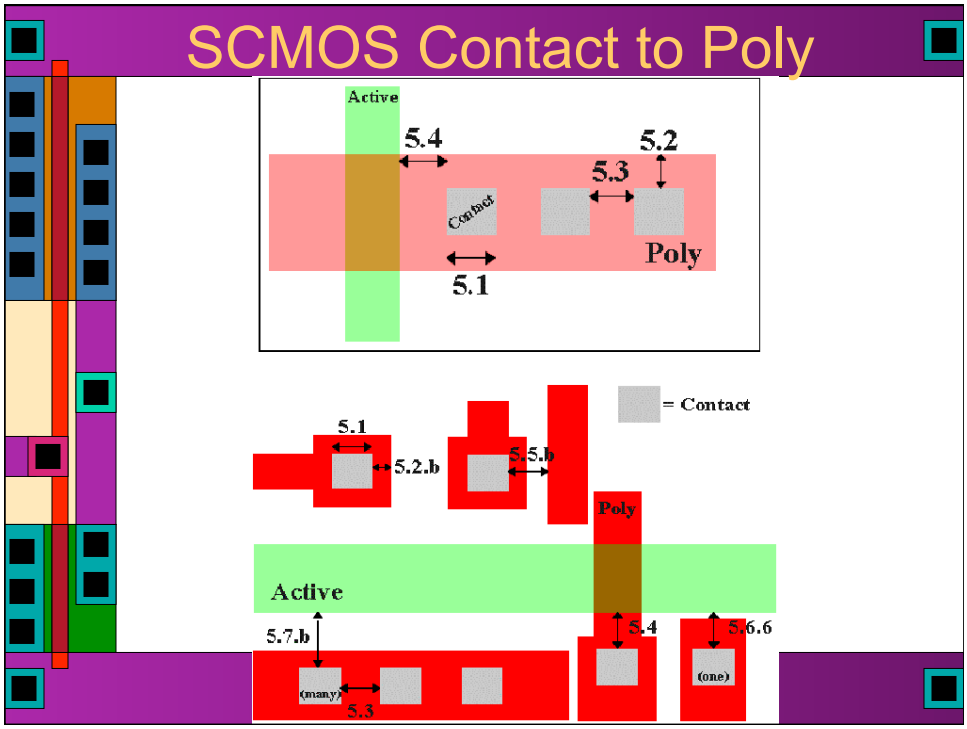
Rule	Description	SUBM	
		SUBM	Microns
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	0.9
4.2	Minimum select overlap of active	2	0.6
4.3	Minimum select overlap of contact	1	0.3
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	0.6

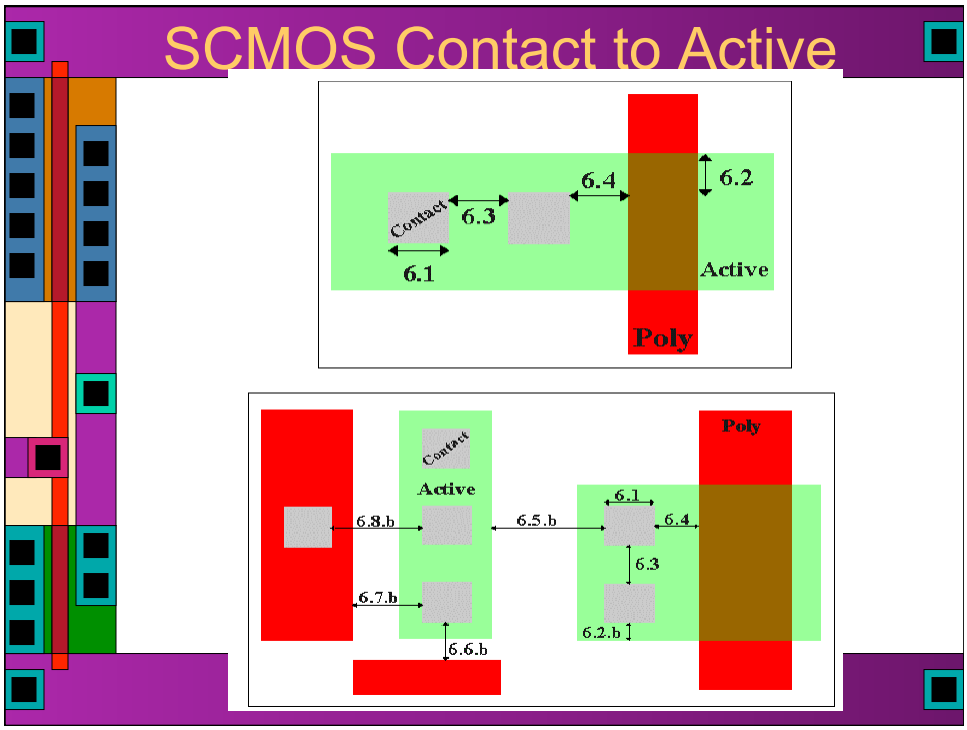


SCMOS Contacts

Rule	Description	SUBM	
		SUBM	Microns
5.1	Exact contact size	2x2	0.6x0.6
5.3	Minimum contact spacing	3	0.9
5.4	Minimum spacing to gate of transistor	2	0.6
5.2.b	Minimum poly overlap	1	0.3
5.5.b	Minimum spacing to other poly	5	1.5
5.6.b	Minimum spacing to active (one contact)	2	0.6
5.7.b	Minimum spacing to active (many contacts)	3	0.9

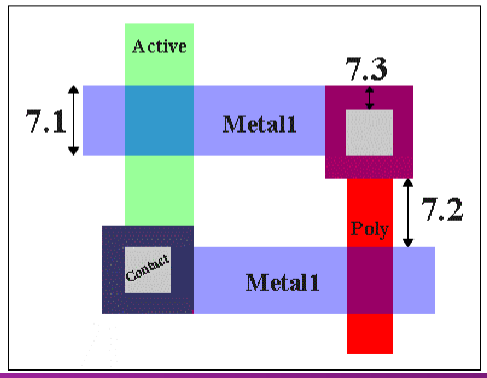
Rule	Description	SUBM	
		Lambda	Microns
6.1	Exact contact size	2x2	0.6x0.6
6.3	Minimum contact spacing	3	0.9
6.4	Minimum spacing to gate of transistor	2	0.6
6.2.b	Minimum active overlap	1	0.3
6.5.b	Minimum spacing to diffusion active	5	1.5
6.6.b	Minimum spacing to field poly (one contact)	2	0.6
6.7.b	Minimum spacing to field poly (many contacts)	3	0.9
6.8.b	Minimum spacing to poly contact	4	1.2


SCMOS Contact to Poly
Active
5.4
5.2
5.3
Contact
Poly
5.1
= Contact
5.1
5.2.b
5.5.b
Poly
Active
5.7.b
5.4
5.6.6
(many)
5.3
(one)


SCMOS Contact to Active
6.4
6.2
Contact
6.3
6.1
Active
Poly
Poly
Contact
Active
6.1
6.3.b
6.5.b
6.4
6.3
6.7.b
6.2.b
6.6.b

SCMOS Metal1

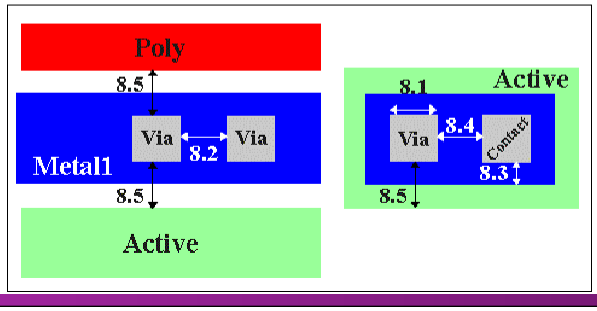
Rule	Description	SUBM	
		Lambda	Microns
7.1	Minimum width	3	0.9
7.2	Minimum spacing	3	0.9
7.3	Minimum overlap of any contact	1	0.3
7.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8



SCMOS Via

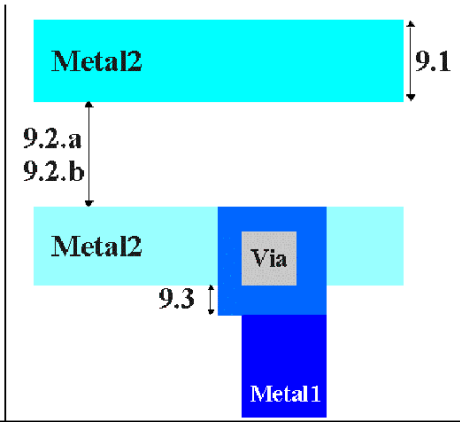
Rule	Description	SUBM	
		3+ Metal Process	
		Lambda	Microns
8.1	Exact size	2 x 2	0.6x0.6
8.2	Minimum via1 spacing	3	0.9
8.3	Minimum overlap by metal1	1	0.3
8.5	Minimum spacing to poly or active edge	2	0.6

Note: Rule 8.4 is not considered for the process we are using since stacked vias are allowed



SCMOS Metal2

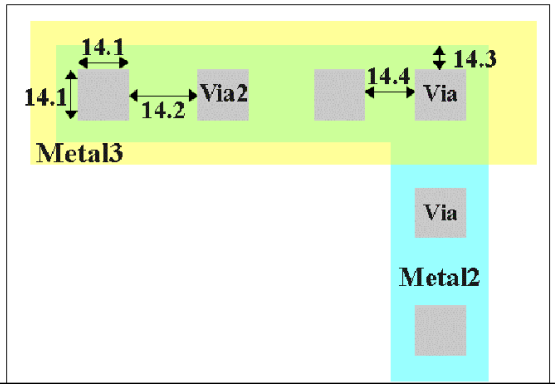
Rule	Description	SUBM 3+ Metal Process	
		Lambda	Microns
9.1	Minimum width	3	0.9
9.2	Minimum spacing	3	0.9
9.3	Minimum overlap of via1	1	0.3
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8



SCMOS Via2

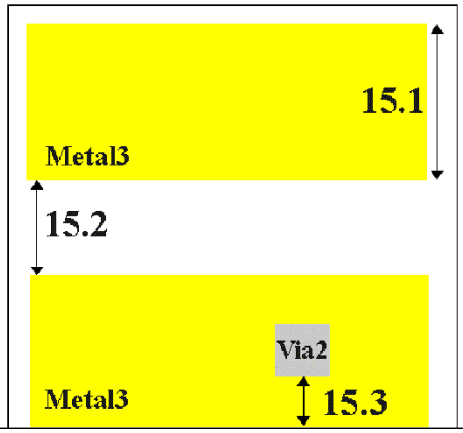
Rule	Description	SUBM 3 Metal Process	
		Lambda	Microns
14.1	Exact size	2x2	0.6x0.6
14.2	Minimum spacing	3	0.9
14.3	Minimum overlap by metal2	1	0.3
14.5	Via2 may be placed over contact		

Note: Rule 14.4 is not considered for the process we are using since stacked vias are allowed

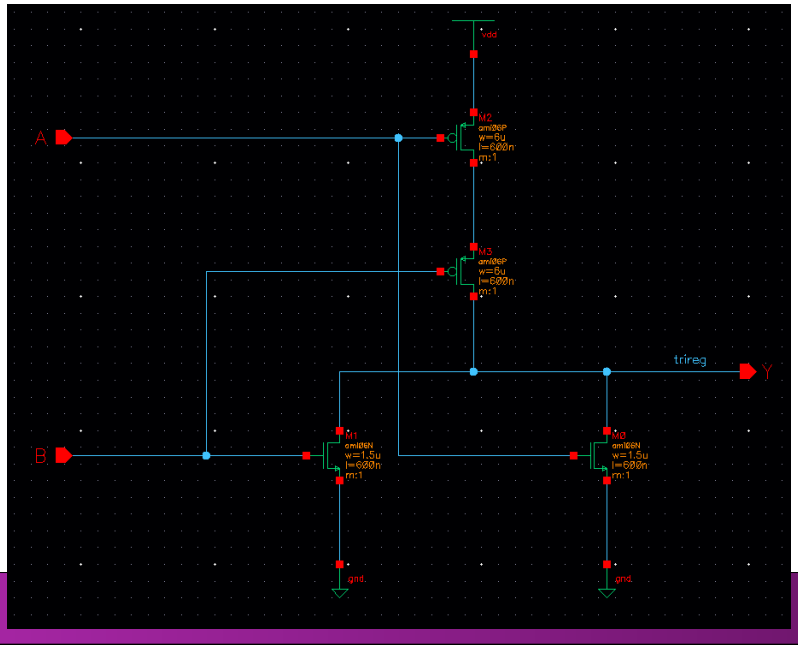


SCMOS Metal3

Rule	Description	SUBM 3 Metal Process	
		Lambda	Microns
15.1	Minimum width	5	1.5
15.2	Minimum spacing to metal3	3	0.9
15.3	Minimum overlap of via2	2	0.6
15.4	Minimum spacing when either metal line is wider than 10 lambda	6	1.8

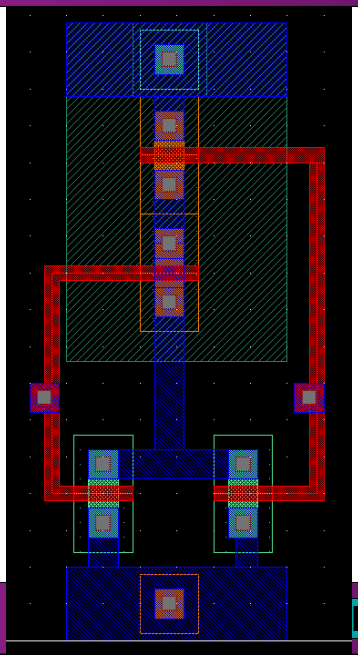


An Example: NOR



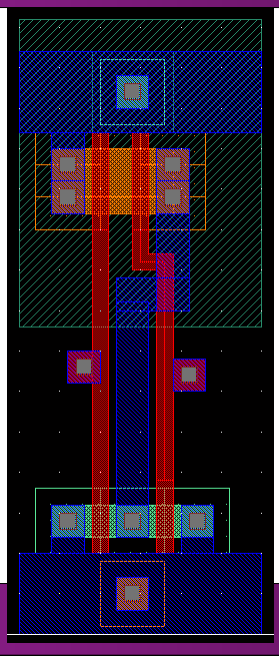
First Layout: Follow Schematic

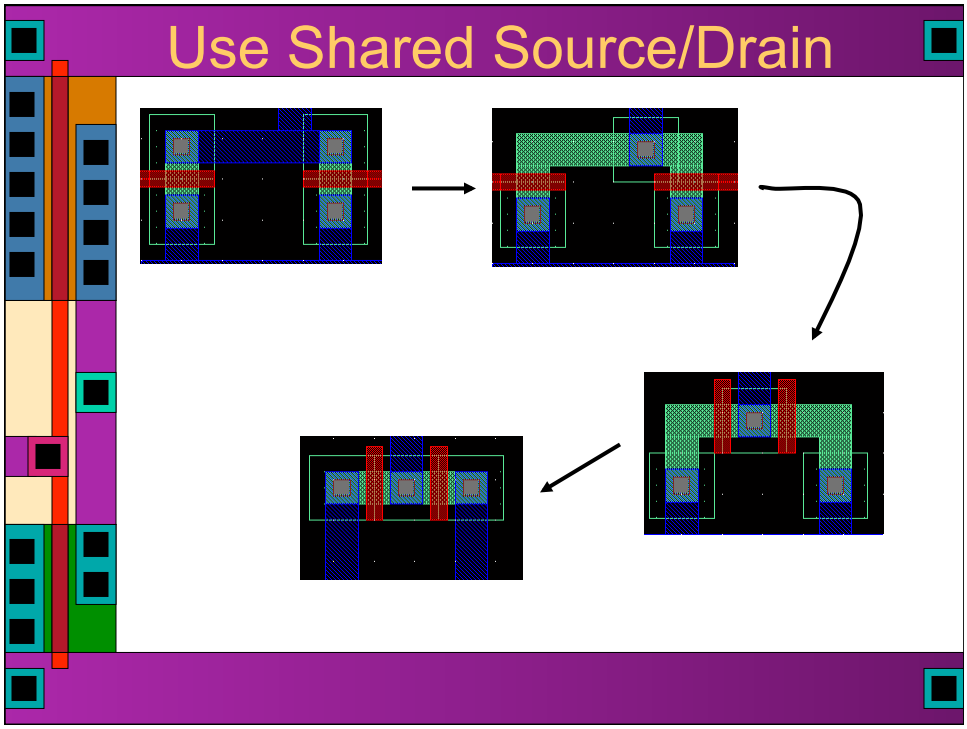
- Note that layout of transistors follows the schematic
  - Two P-types in series pulling up
  - Two N-types in parallel pulling down

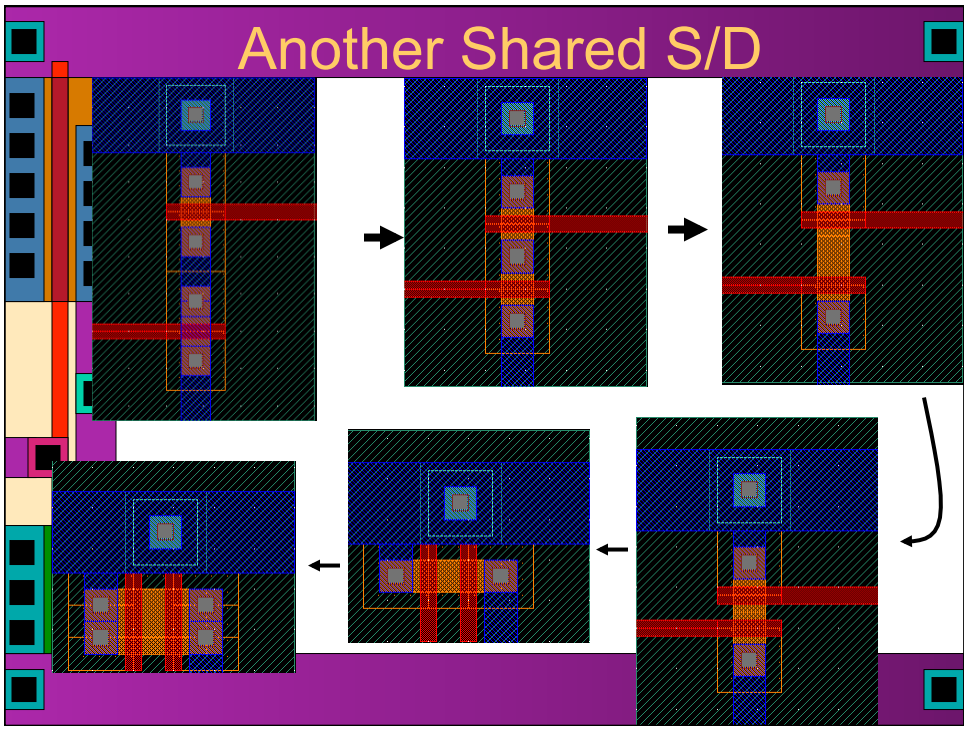


Another Layout: Better?

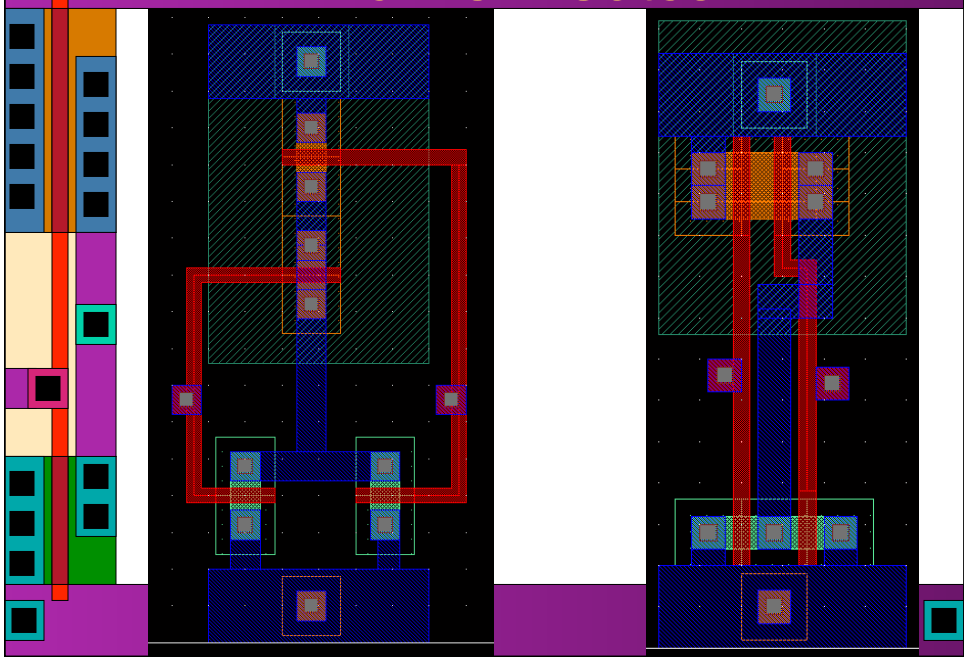
- Same four transistors
  - But, organized a little differently
  - And sized a little differently




Use Shared Source/Drain

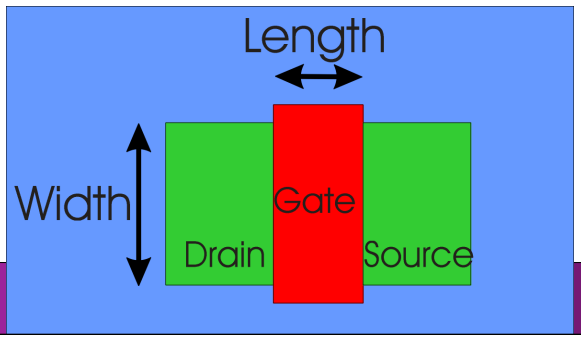

Another Shared S/D

Two NOR Gates



Transistor Sizing

- We'll get into the details later…
- Consider a transistor's Width and Length
  - Current capability is proportional to W/L
  - Length is almost always minimum allowed
  - Change width to change current capability



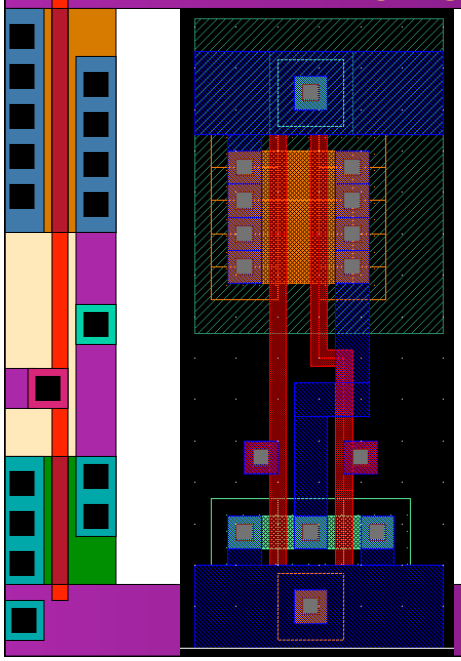
Sizing Rule of Thumb

- Also, P-type is about twice as bad as N-type
  - Has to do with hole mobility vs. electron mobility
- So, make P-types twice as wide as N-types to start with
- Unit size for transistors this semester
  - N-type 1.5μ (contact pitch is 1.2μ)
  - P-type 3μ

Sizing Rule of Thumb

- Now multiply each width by n for a series stack of n transistors.
  - Stack of 2 in series, each transistor should be 2x unit size
  - Stack of 3 in series, each transistor should be 3x unit size
- This is because series connections are like increasing the L of the device…
  - Current is proportional to W/L

For example:



- Notice the difference in width…
- This roughly equalizes the current sourcing capability of pull-up and pull-down stacks in this gate