Chip Assembly

Using the
Virtuoso Chip Assembly Router
(vcar)

Yet Another Tool...

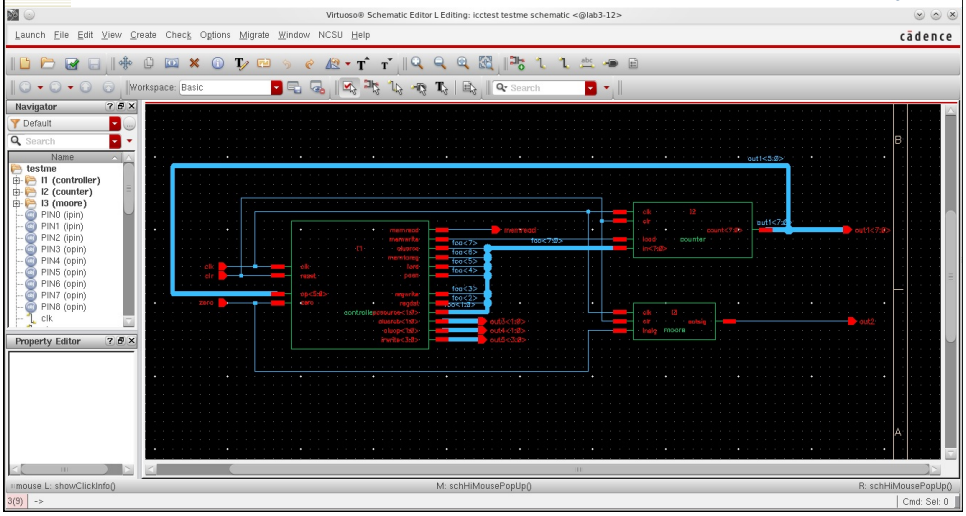
- This is a tool you can use to connect large blocks that have been designed separately
  - Like placed and routed blocks from SoC, or memories, or custom register files, etc.
- Also useful for wiring a fully-connected core to the pads
- Hand-placement, but automated wiring...
- Chapter 12 in CAD book

Outline

1. Start with a schematic to define connectivity
2. Then generate a layout template into Virtuoso-XL
3. Place blocks by hand and adjust floorplan
4. Wire vdd and gnd by hand
5. Export to vcar for signal routing
6. Import back into Virtuoso for DRC, LVS, GDS

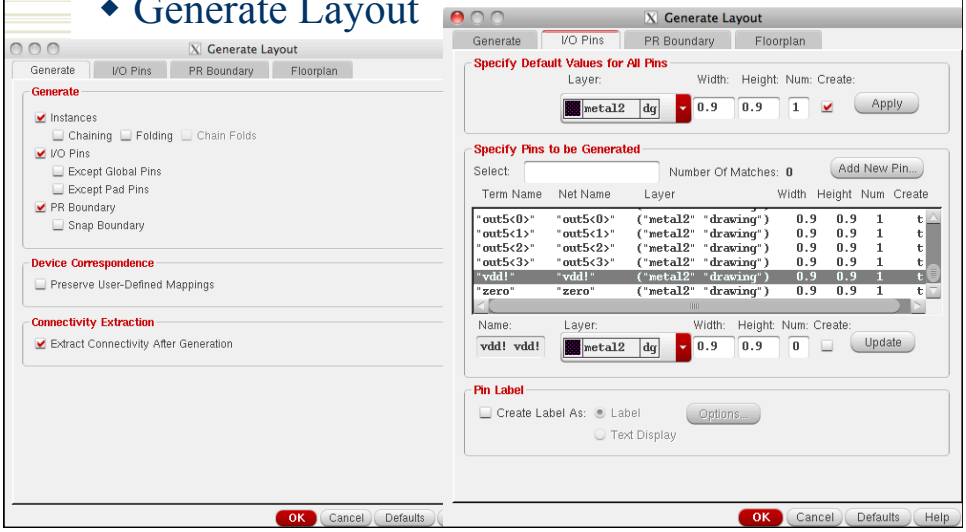
Example

- Start with schematic that defines connectivity



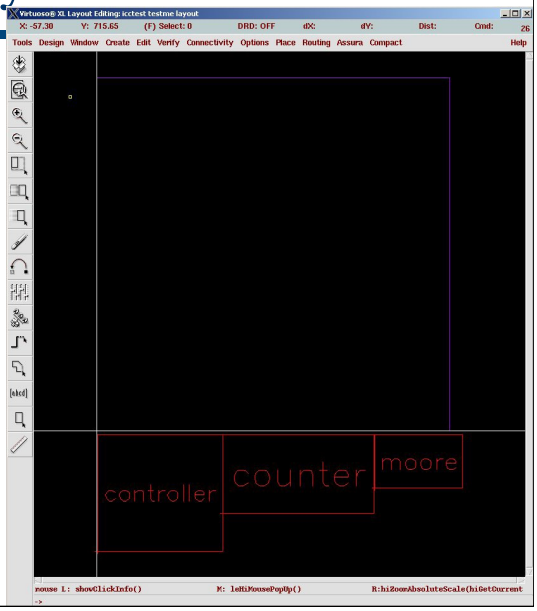
Generate layout from schematic

- Generate Layout

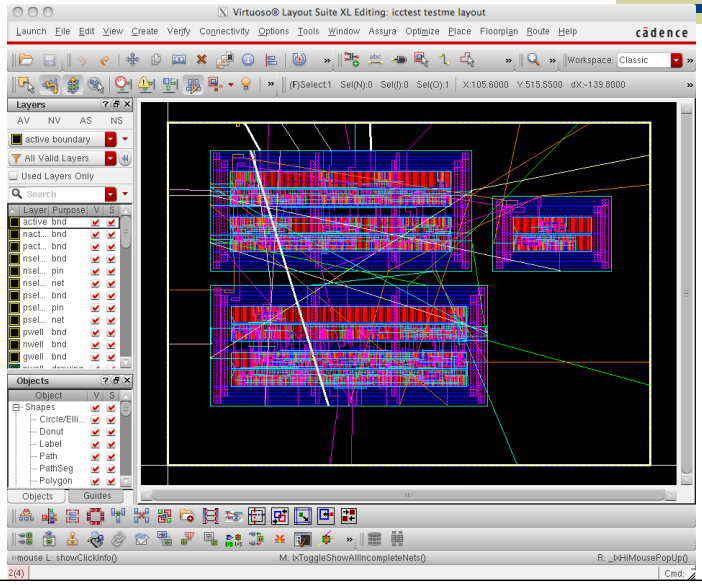


Generate layout from schematic

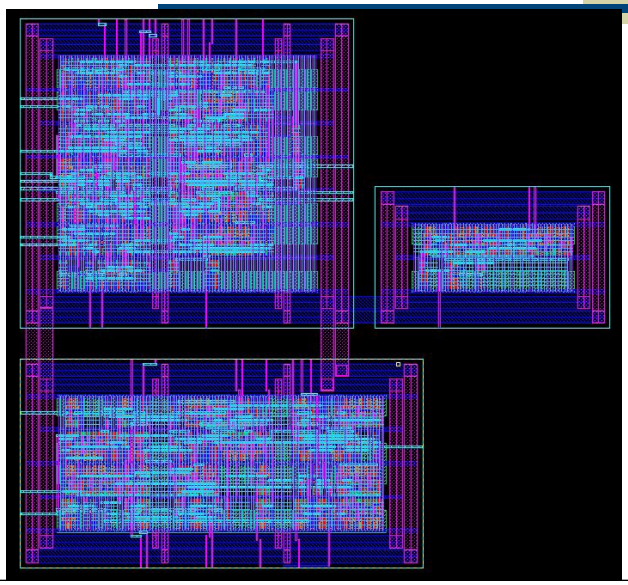
- Generate Layout



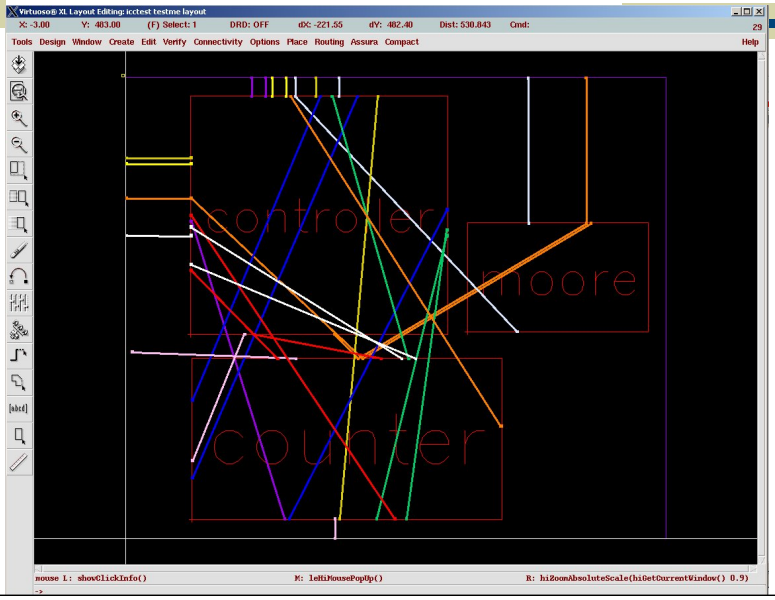
Drag to place floorplan



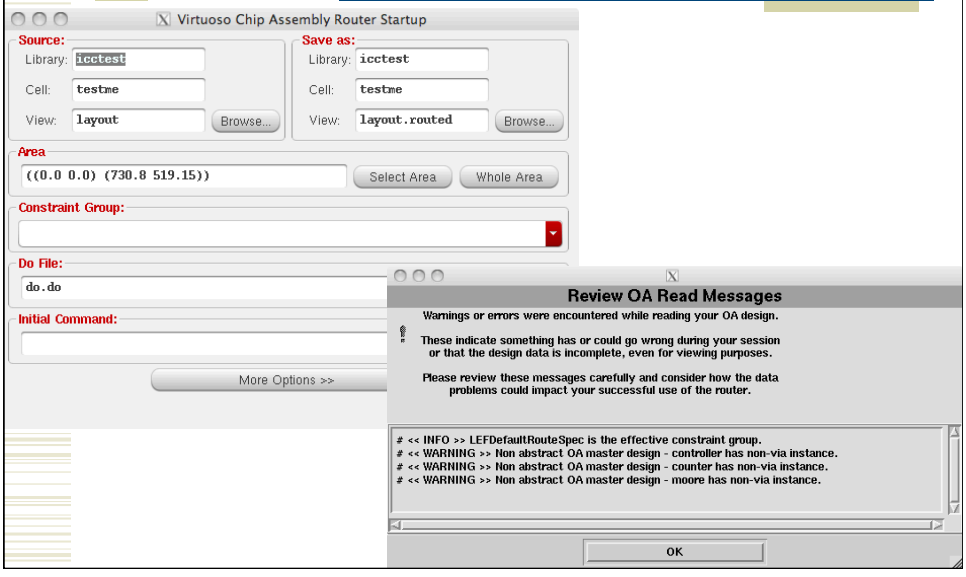
Floorplan before routing



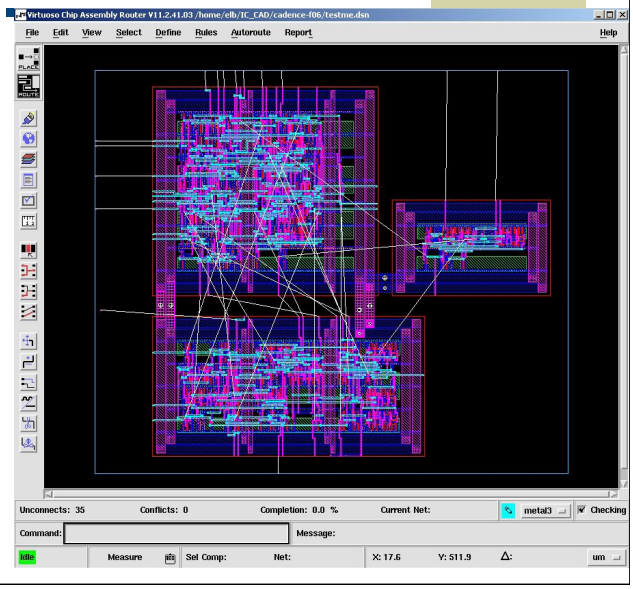
View with just Flight Lines



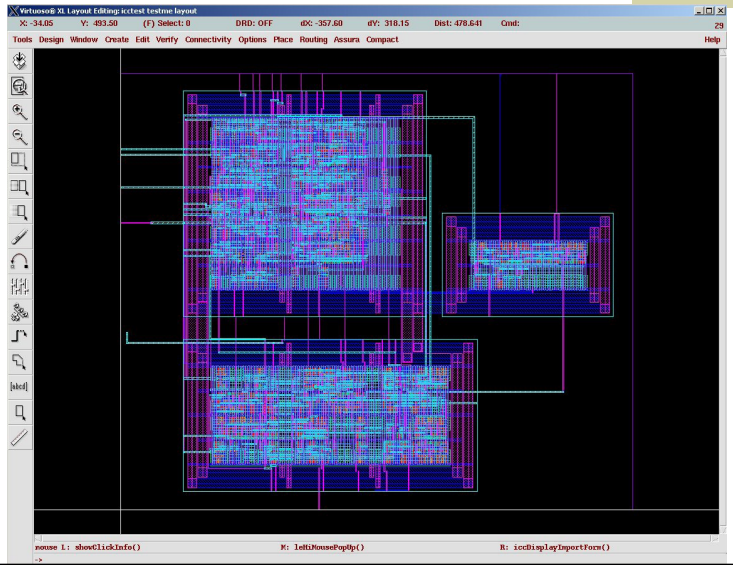
Export to vcar



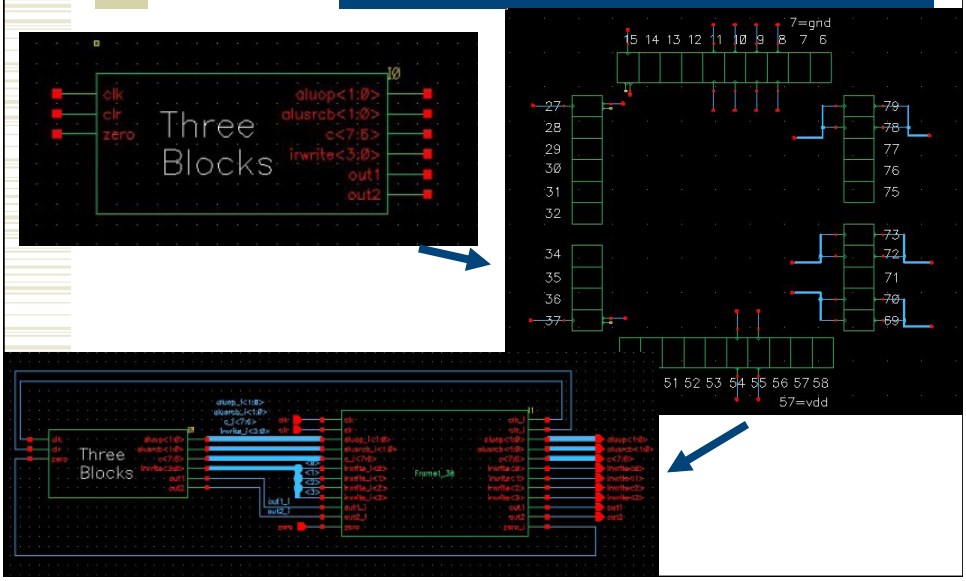
Export to vcar



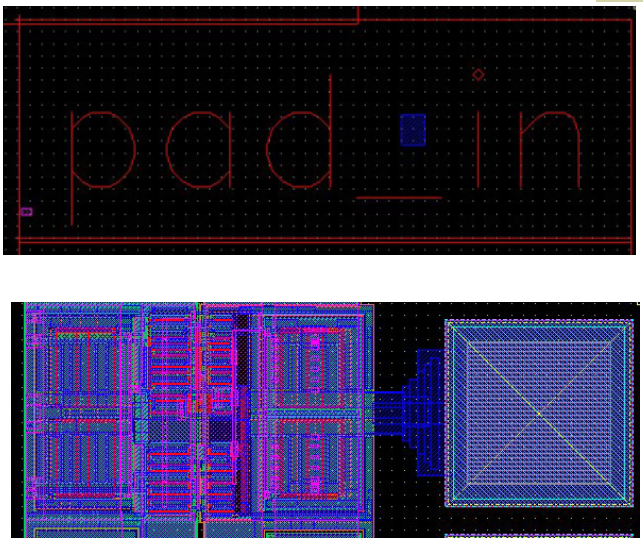
Layout after routing



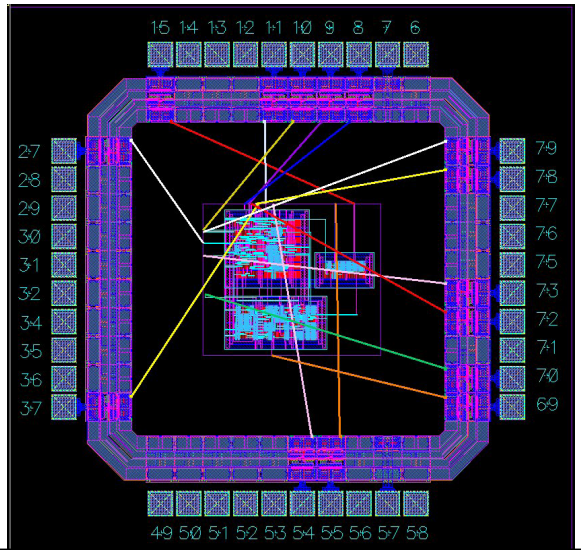
Example of Core to Pad Routing



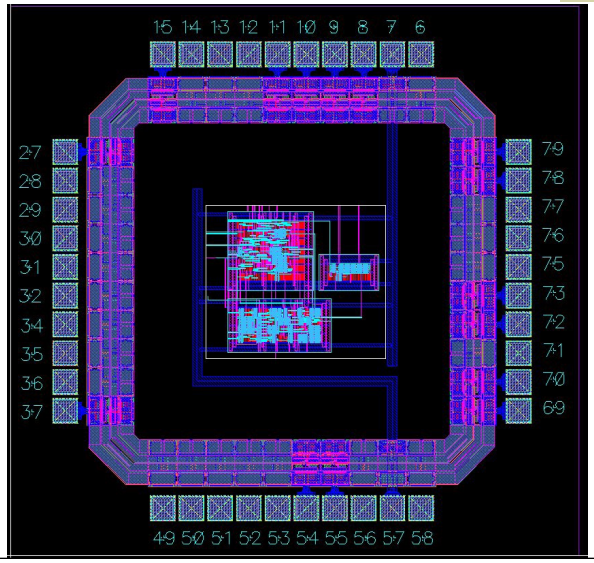
Example Pins on Pad (layout)



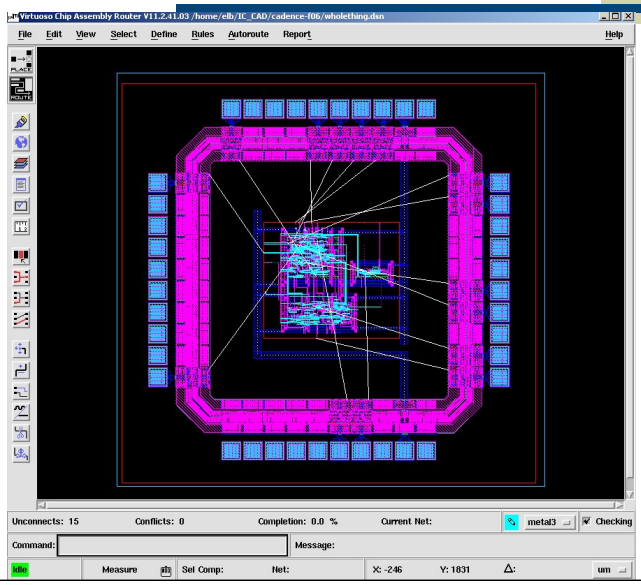
Core and Frame in Virtuoso-XL



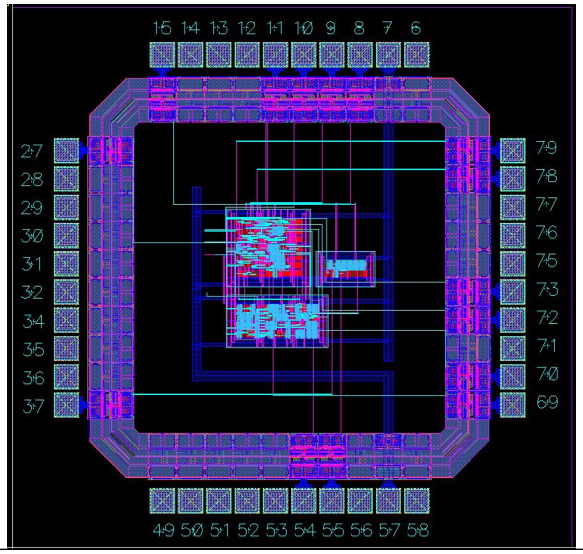
Make Vdd and Gnd connections



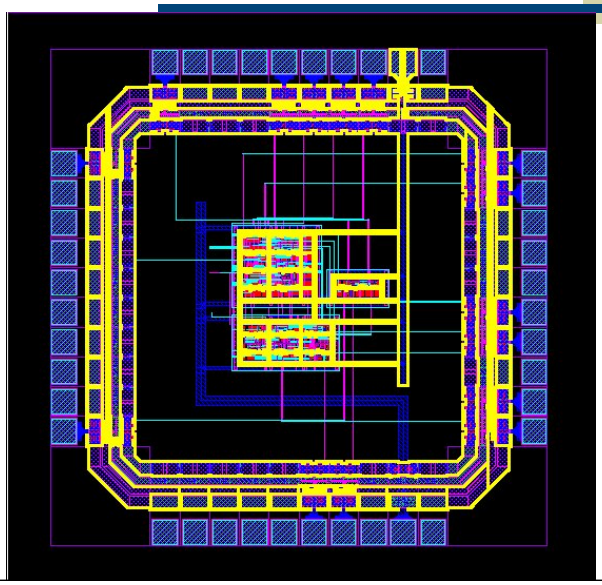
Send to vcar



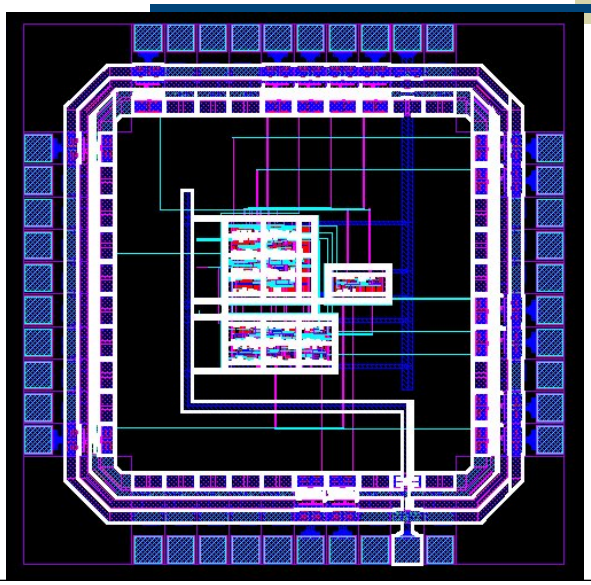
After vcar routing



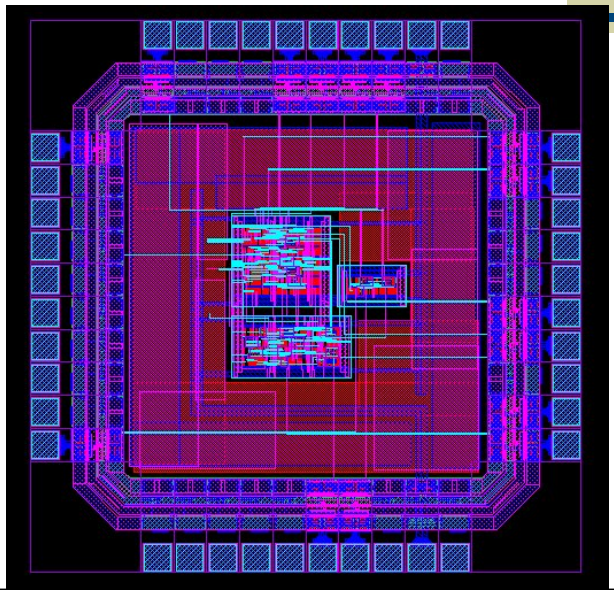
Check GND



Check VDD

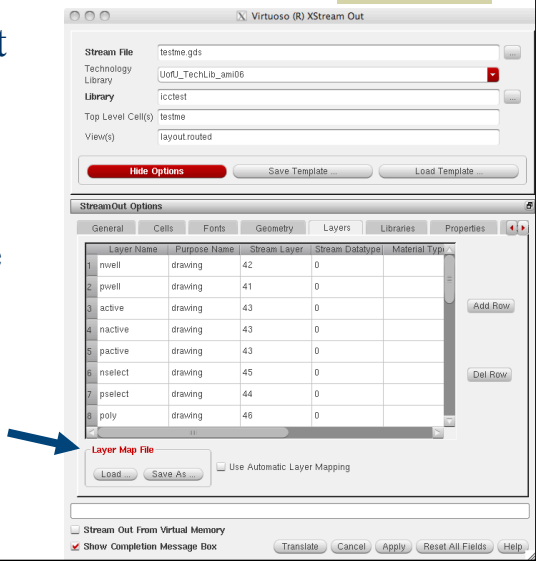


Add Fill



Now generate gdsII (stream)

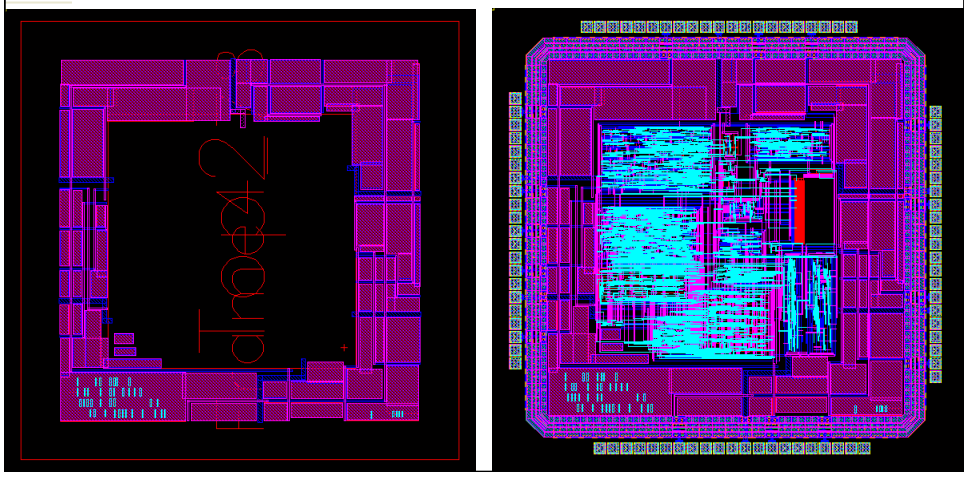
- The binary format that MOSIS wants
- Use export->stream
  - Make sure to load stream4gds.map as the Layer Map File



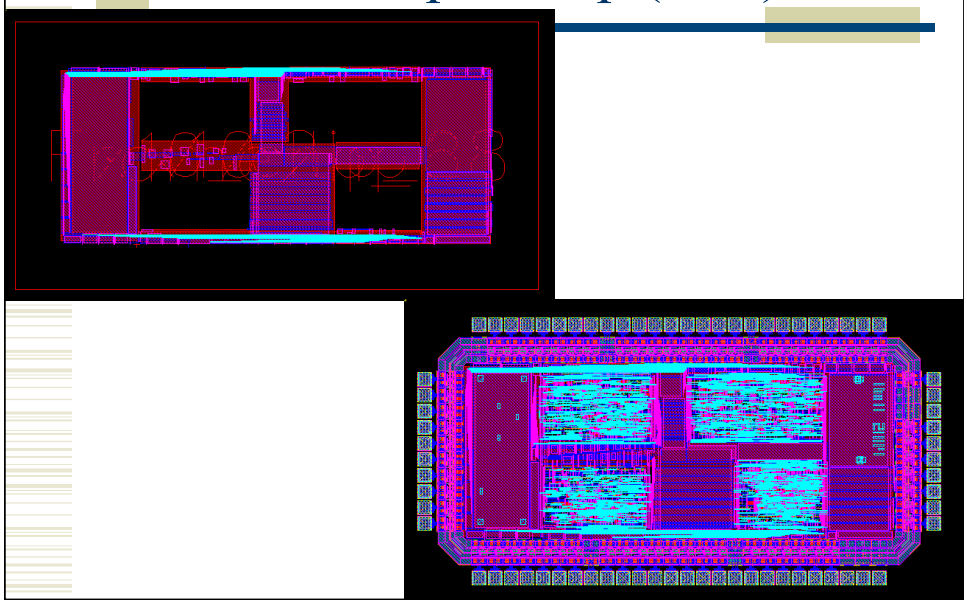
One Final Tweak

- If you're fabbing, before you generate your final fab-read gdsII (stream) file...
  ...You need to add blocks of poly, M1, and M2 to meet the minimum density requirements
  - Take open areas of your chip and add large blocks of those layers
  - Remember to DRC and LVS to make sure you didn't mess anything up!

Example Chip (4tcu)



Example Chip (2tcu)



Example Chip (1tcu)