CS/EE 5710/6710 — Digital VLSI Design

Example Midterm

Name:

Instructions This is a closed-book, closed-notes exam. I want to see what you've learned by coming to lectures, reading, and working on your project, not what you can look up in the textbook. The subjects of the questions are things that I think you should know having been involved in the class to this point.

Work independently. Show your work! Answers with no justification will not be given credit. *Don't Panic!*

Put your name at the top of each sheet of the exam before you start!

1	10 points	
2	24 points	
3	18 points	
4	18 points	
5	15 points	
6	15 points	
Total	100 points	

1 Multiple Choice Questions: 10 points

Choose the one best answer:

a. Which of the following is true for an nmos transistor operating in its *linear* or *triode* mode? (Vgs = gate to source voltage, Vds = drain to source voltage, Vt = threshold voltage)

   (a) Vds $<$ (Vgs - Vt)
   (b) Vds $>$ (Vgs - Vt)
   (c) Vgs $<$ Vt
   (d) Vgs = 0v

b. Which of the following would result in the *strongest* transistor (lergest β)?

   (a) nmos w=3μ l=0.6μ
   (b) nmos w=0.6μ l=3μ
   (c) pmos w=3μ l=0.6μ
   (d) pmos w=0.6μ l=3μ

c. The capacitance of a transistor gate is proportional to what?

   (a) The width of the gate
   (b) The length of the gate
   (c) The area of the gate
   (d) The depth of the channel

d. The *hold time* of a sequential device (like a flip flop) is defined to:

   (a) Ensure that the next stage is ready to receive data.
   (b) Ensure that the data are not removed too soon after the clock is applied
   (c) Ensure that the input data have settled before the clock is applied.
   (d) Ensure that the outputs change at the proper time.

e. Which of the following processing techniques would be used to create the source and drain regions of a transistor?

   (a) Oxidation
   (b) Ion implantation
   (c) Sputtering
   (d) Polysilicon deposition

2 Short Answer Questions: 24 Points

Please answer the questions concisely. I'm not looking for a dissertation on each subject, just a brief description of the important ideas.

2.1 6 points

Our "standard" sizes for transistors start with a basic width, and then multiply that width by the number of devices in series in that stack. For example, if you have three nmos transistors in series, we multiply their basic width by 3 to get our "standard" width. Why?

2.2 Circuit Characterization: 6 points

What is meant by "rise resistance" in a characterization of a cell for synopsys? How does it relate to cell timing?

(Fall 2009) Note that this an old question and isn't related to the table-driven characterization technique that we use with ELC.

2.3 Logical Effort: 6 points

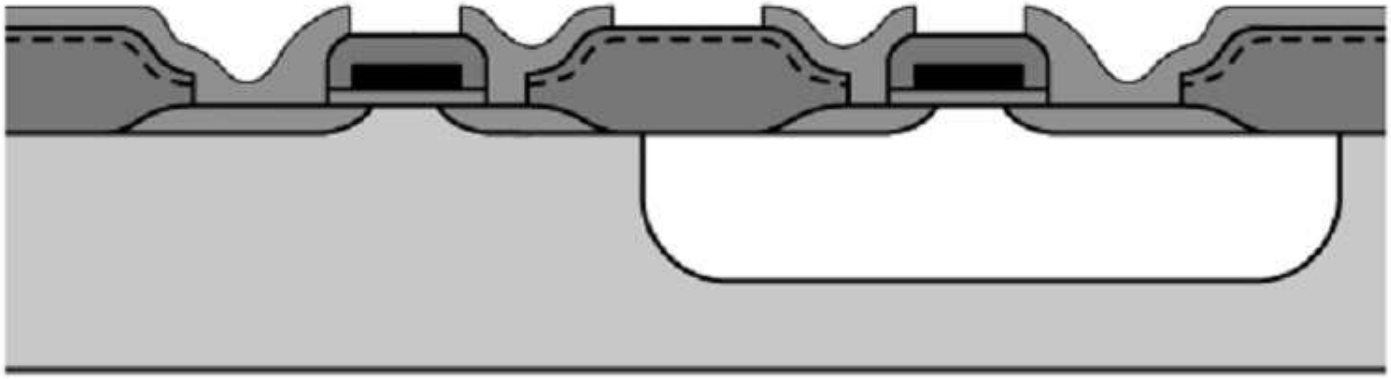
How would you go about using Logical Effort to design a circuit that starts with a unit-sized inverter (1.5u nmos and 3u pmos) and that eventually has to drive a load 100 times as large as the unit inverter's input load? You don't need to solve the equations, just describe the design process and the important concepts.

2.4 6 points

Describe the main three sources of power dissipation in static CMOS circuts. Which is the most dominant source of power dissipation in today's circuits? What about future circuits in processes with deep sub-micron gate lengths?

2.5 Processing: 18 points

The diagram below is a cross section of a CMOS circuit with one N-type and one P-type transistor. Identify one example of each of the following layers in the diagram: NWELL, N-active, field oxide, gate oxide, polysilicon, metal1.



3 Circuit Design: 18 points

Design a single complex static CMOS gate (i.e. one pullup network and oue pulldown network, not a tree of pre-designed gates) that implements the following function. You can assume that inverted versions of the input literals are available (i.e. you don't have to draw the inverters for inverted inputs). In particular:

a. Draw a minimized transistor level schematic for the complex gate (use the fewest possible transistors)

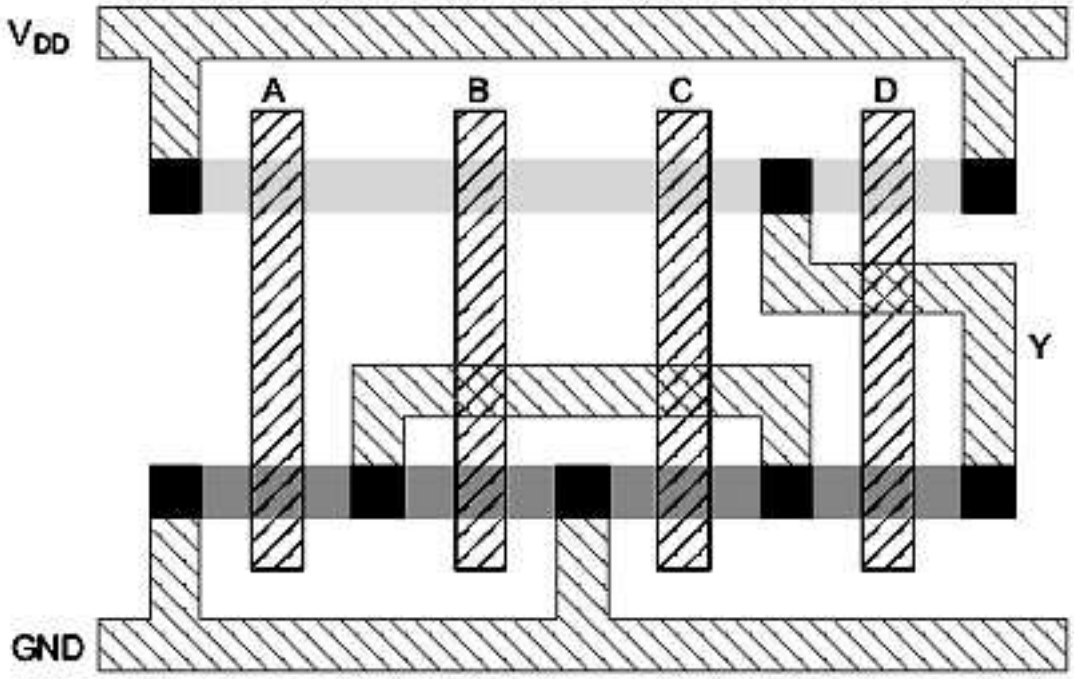
b. Draw an Euler diagram and use it to choose a variable ordering for a line-of-diffusion style layout

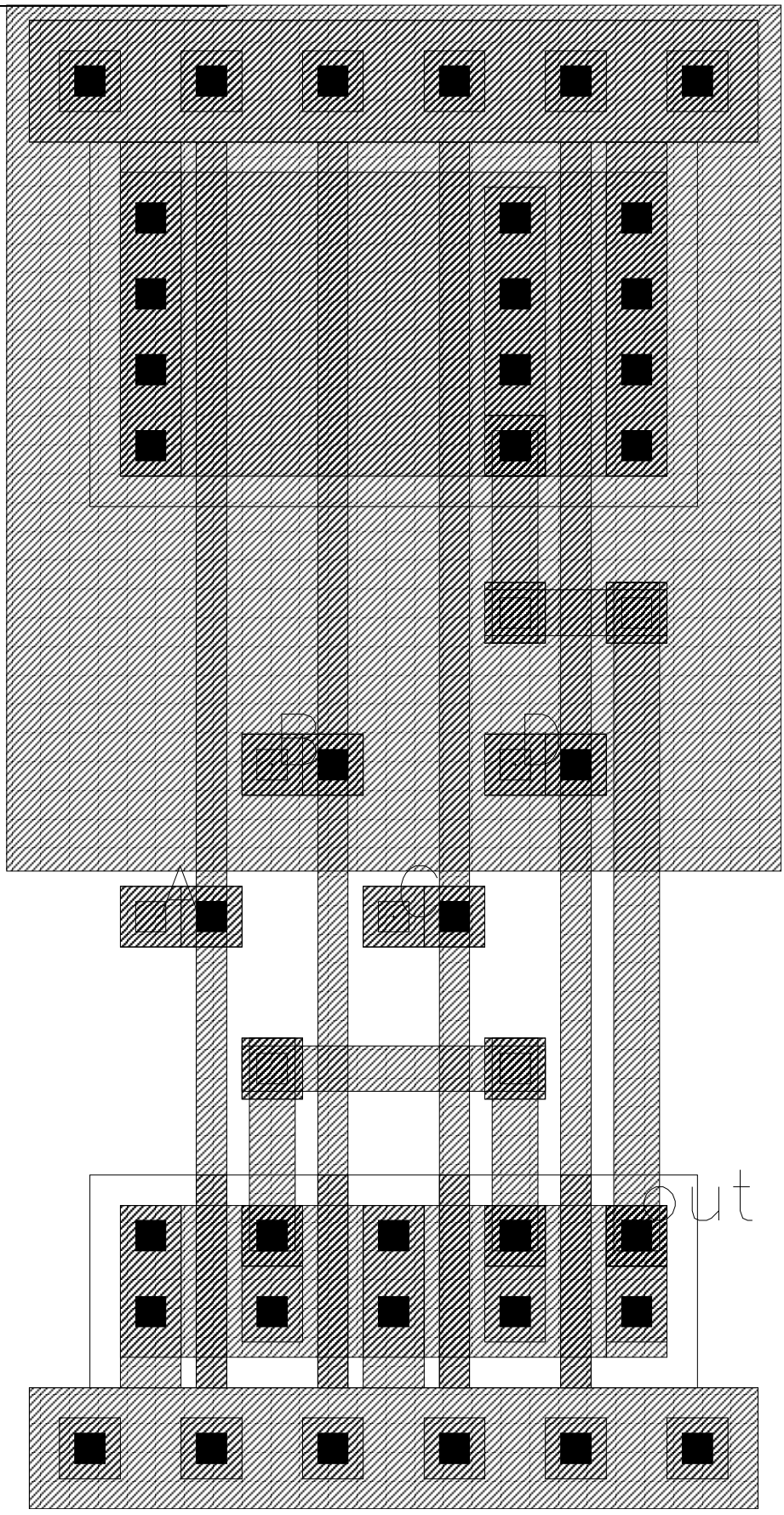
c. Draw a stick diagram of a layout using that variable ordering

$$F = A\,C\,D\; + A\,B\,\overline{D}$$

3.1 Layout Design: 15 points

What function is performed by the following CMOS layout? Extract and draw the transistor schematic of the circuit, and define the function as a Boolean expression. The circuit is shown as a stick diagram of the type in the text book on this page with the P-type transistors on the top and the N-type transistors on the bottom. It is also shown as a Cadence layout on the following page. They are the same circuit, just different views.




A
B
out

3.2 Verilog Testbench Code: 15 Points

For the function on the previous problem, write a self-testing testbench file in Verilog that tests for the following three patterns only (i.e. not exhaustive): ABCD = 0000, 0101, 1010. Your Verilog testbench should report errors if they appear. The testbench shell as it would appear in Verilog-XL is given.

```
\\ Default verilog header - add your own code after this...
initial
begin
   A = 1'b0;
   B = 1'b0;
   C = 1'b0;
   D = 1'b0;




end
```