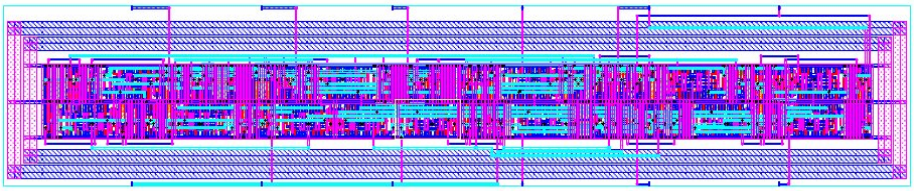
CS/ECE 5710/6710
Digital VLSI Design



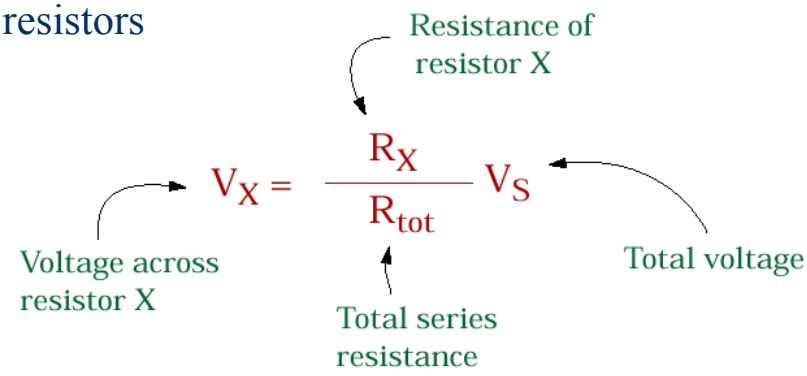
Electronics Summary

- Voltage is a measure of electrical potential energy
- Current is moving charge caused by voltage
- Resistance reduces current flow
  - Ohm's Law: $V = I R$
- Power is work over time
  - $P = I V = I^2R = V^2/R$
- Capacitors store charge
  - It takes time to charge/ discharge a capacitor
  - Time to charge/discharge is related exponentially to RC
  - It takes energy to charge a capacitor
  - Energy stored in a capacitor is $(1/2)CV^2$

Energy (joules): work required to move one coulomb of charge by one volt or work done to produce one watt for one sec

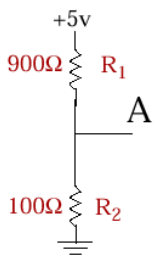
Reminder: Voltage Division

- Find the voltage across any series-connected resistors

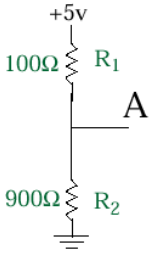


Example of Voltage Division

- Find the voltage at point A with respect to GND



$$V_X = \frac{R_X}{R_1 + R_2} V$$



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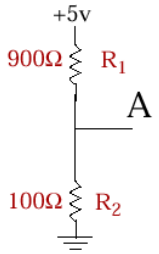

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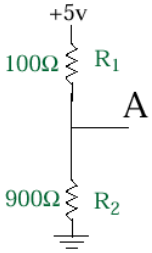


$V_1 = (900/1000)\ 5v = 4.5v$
$V_2 = (100/1000)\ 5v = 0.5v$

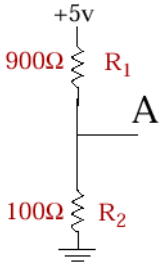
So, $V_{A\text{-}GND} = 0.5v$

$V_1 = (100/1000)\ 5v = 0.5v$
$V_2 = (900/1000)\ 5v = 4.5v$

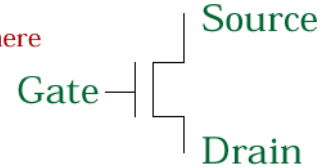
So, $V_{A\text{-}GND} = 4.5v$

How Does This Relate to VLSI?

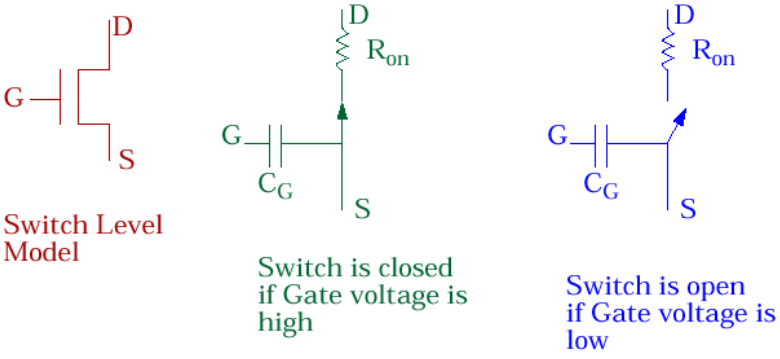
- Recall the voltage division example:
  - Consider what we could do if we had a device that we could switch from high resistance to low resistance
  - We could use it to force A high or low depending on the relative resistance of the elements



- This is a transistor
  - Specifically a CMOS FET
  - Complementary Metal-Oxide Semiconductor Field Effect Transistor
  - If voltage on Gate is high, then there is a low-resistance between Source and Drain, otherwise it's a very high-resistance



Model of a CMOS Transistor



Switch Level Model

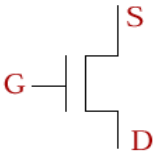
Switch is closed if Gate voltage is high

Switch is open if Gate voltage is low

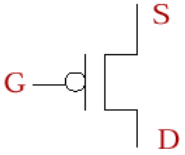
R_{on} = Some resistance in FET itself
C_G = Capacitance of the gate

Two Types of CMOS Transistors

- N-type transistor
  - High voltage on Gate connects Source to Drain
  - Passes 0 well, passes 1 poorly



- P-type transistor
  - Low voltage on Gate connects Source to Drain
  - Passes 1 well, passes 0 poorly

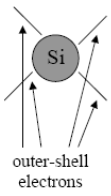


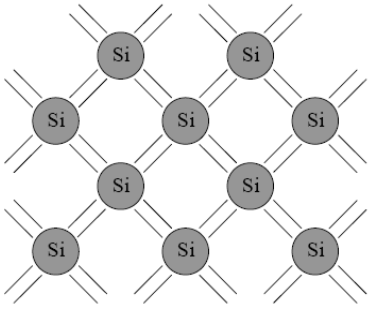
CMOS Transistors

- Complementary Metal Oxide Semiconductor
- Two types of transistors
  - Built on silicon substrate
  - "majority carrier" devices
  - Field-effect transistors
    - An electric field attracts carriers to form a conducting channel in the silicon…
    - We'll get much more of this later…
    - For now, just some basic abstractions

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors

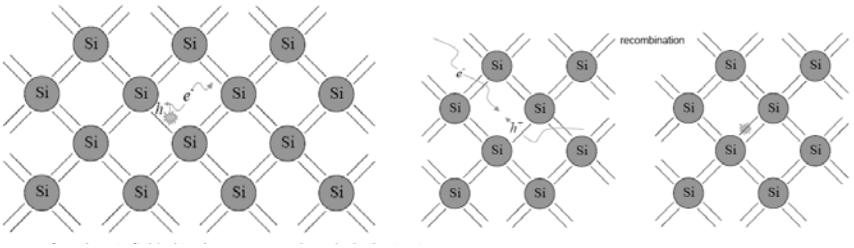




Figures from Reid Harrison

"Semi" conductor?

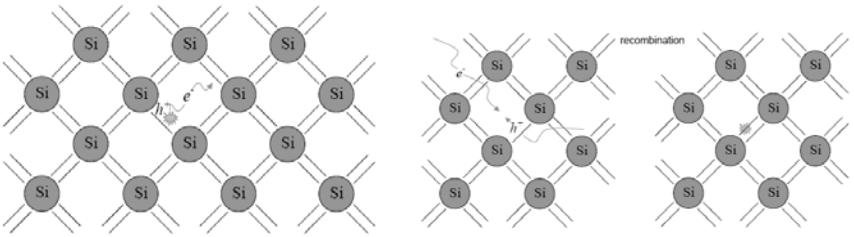
- Thermal energy (atomic-scale vibrations) can shake an electron loose
  - Leaves a "hole" behind



Figures from Reid Harrison

"Semi" conductor?

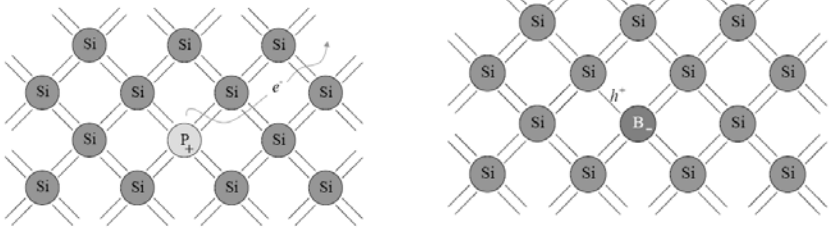
- Room temperature: 1.5×10^{10} free electrons per cubic centimeter
  - But, 5×10^{22} silicon atoms / cc
  - So, one out of every 3 trillion atoms has a missing e



Figures from Reid Harrison

Dopants

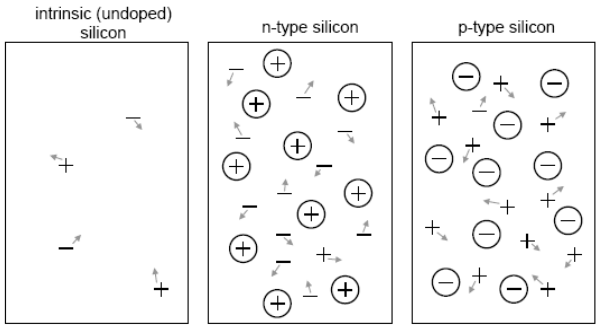
- Group V: extra electron (n-type)
  - Phosphorous, Arsenic,
- Group III: missing electron, (p-type)
  - Usually Boron



Figures from Reid Harrison

Dopants

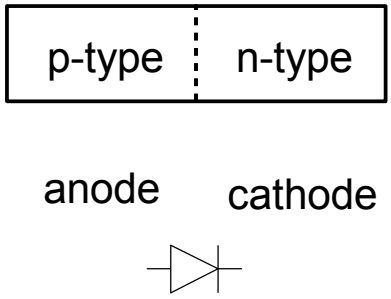
- Note that each type of doped silicon is electrostatically neutral in the large
  - Consists of mobile electrons and holes
  - And fixed charges (dopant atoms)



Figures from Reid Harrison

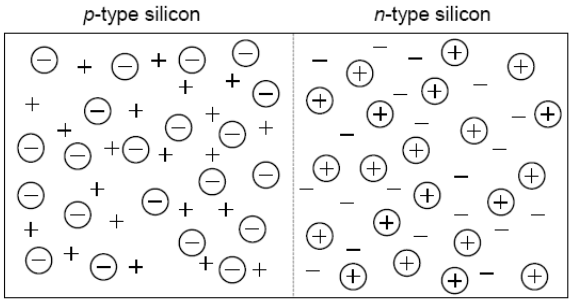
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
  - Current flows only in one direction



p-n Junctions

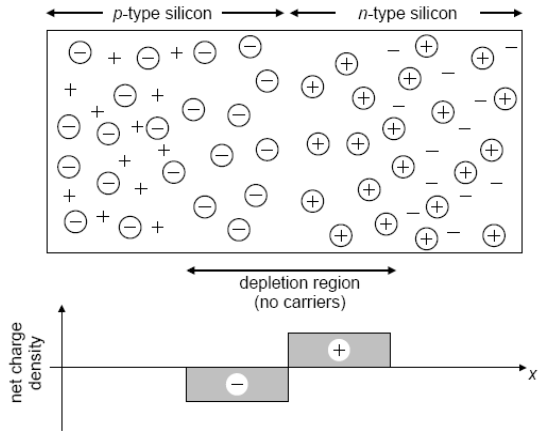
- Two mechanisms for carrier (hole or electron) motion
  - Drift - requires an electric field
  - Diffusion – requires a concentration gradient



Figures from Reid Harrison

p-n Junctions

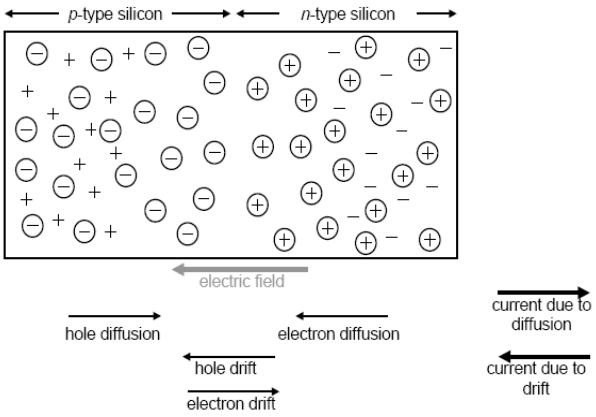
- With no external voltage diffusion causes a depletion region
  - Causes an electric field because of charge recombination
  - Causes drift current…



Figures from Reid Harrison

p-n Junctions

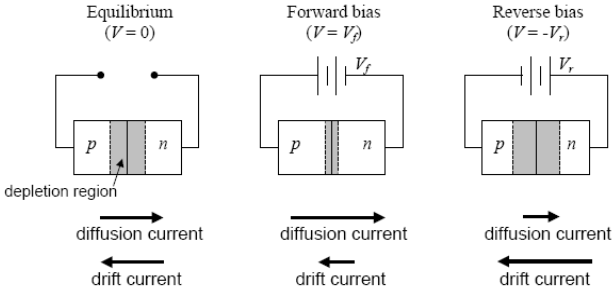
- Eventually reaches equilibrium where diffusion current offsets drift current



Figures from Reid Harrison

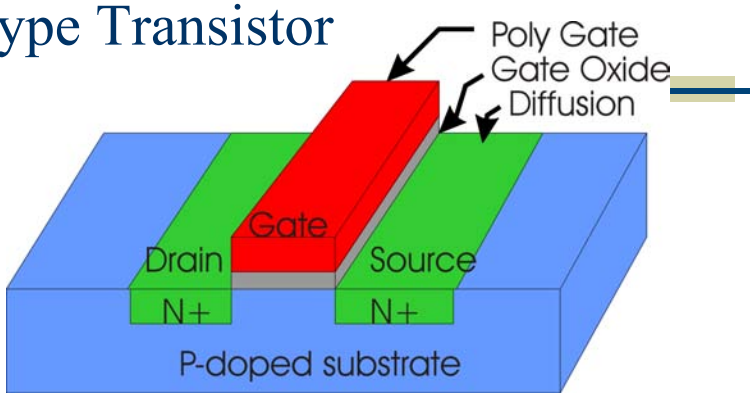
p-n Junctions

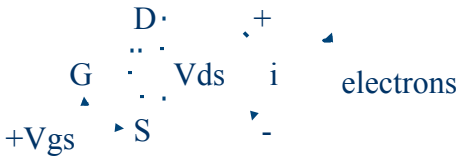
- By applying an external voltage you can modulate the width of the depletion region and cause diffusion or drift to dominate…



Figures from Reid Harrison

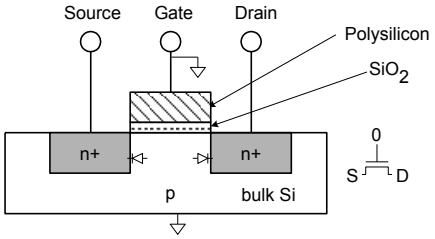
N-type Transistor





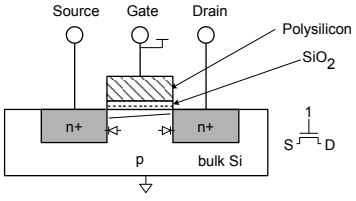
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF

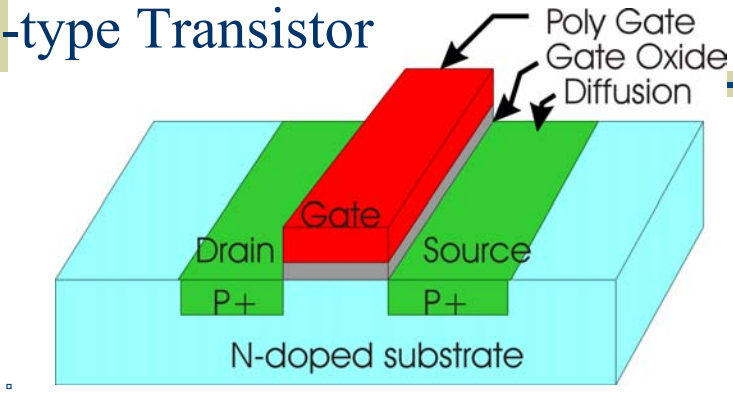


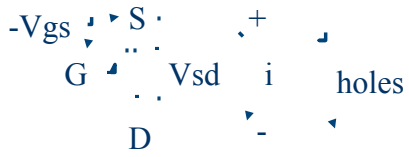
nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



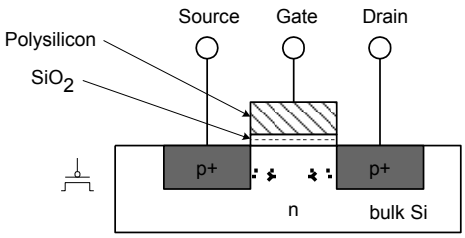
P-type Transistor





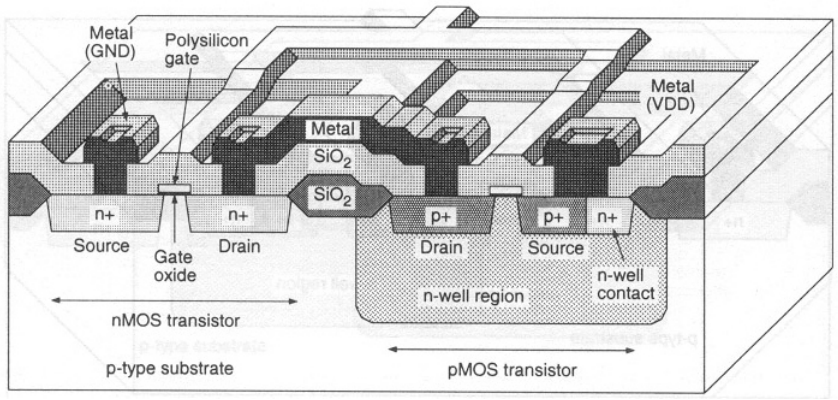
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



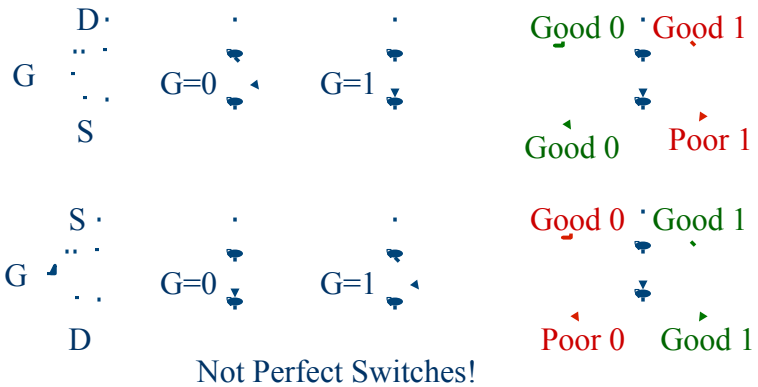
A Cutaway View

- CMOS structure with both transistor types



Transistors as Switches

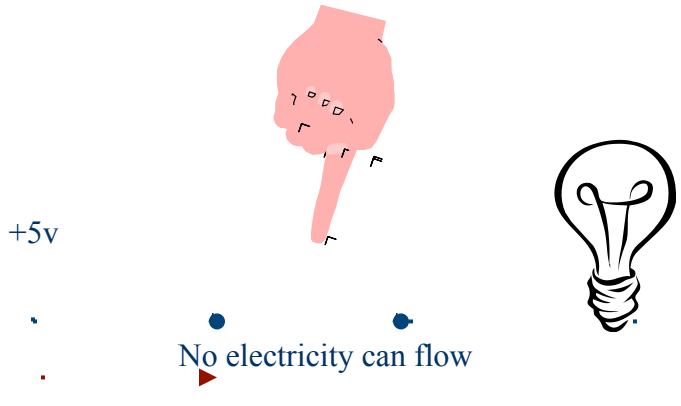
- For now, we'll abstract away most analog details…



Not Perfect Switches!

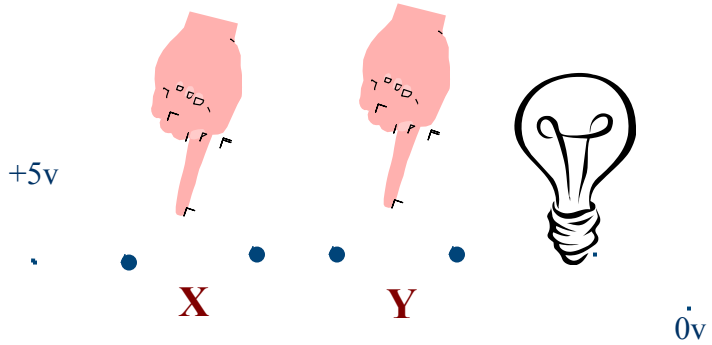
"Switching Circuit"

- For example, a switch can control when a light comes on or off



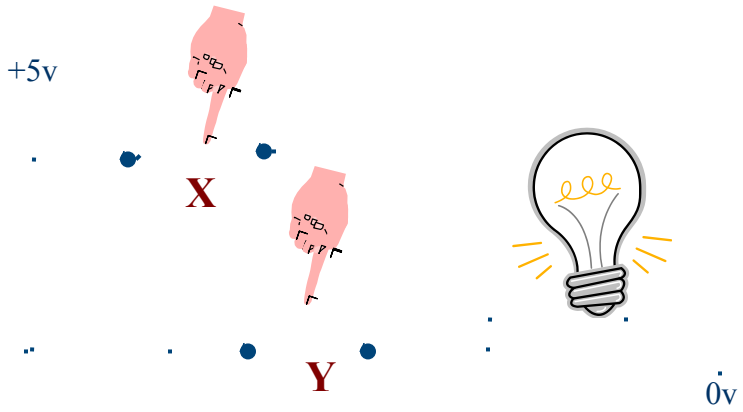
"AND" Circuit

- Both switch **X** **AND** switch **Y** need to be closed for the light to light up



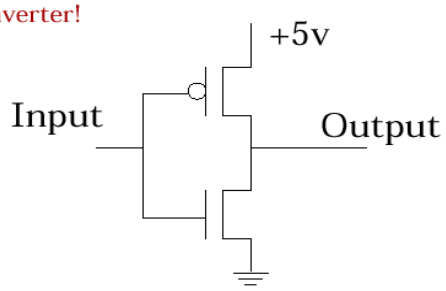
"OR" Circuit

- The light comes on if either **X OR Y** are closed



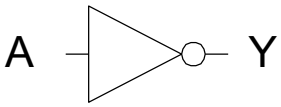
CMOS Inverter

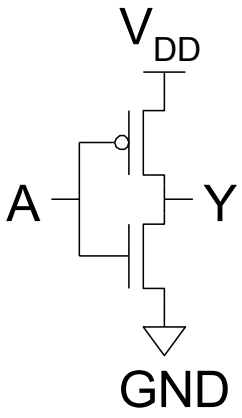
- Consider this connection of transistors
  - If input is at a high voltage, output is low
  - If input is at a low voltage, output is high
- By changing the resistances, it becomes one of two different voltage dividers
  - It's a voltage inverter!



CMOS Inverter

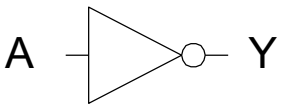
A	Y
0	
1	

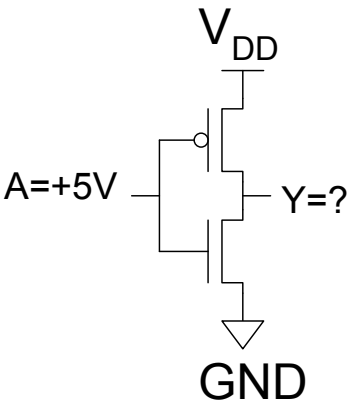




CMOS Inverter

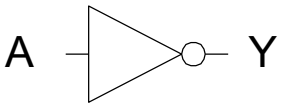
A	Y
0	
1	?

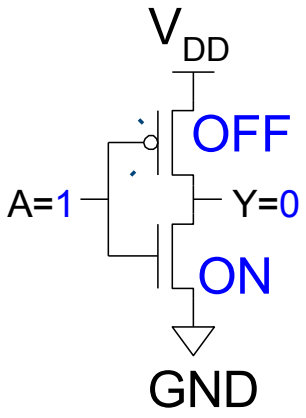




CMOS Inverter

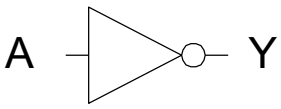
A	Y
0	
1	**0**

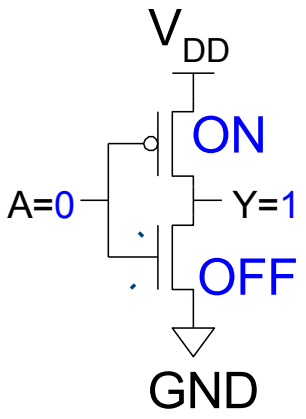




CMOS Inverter

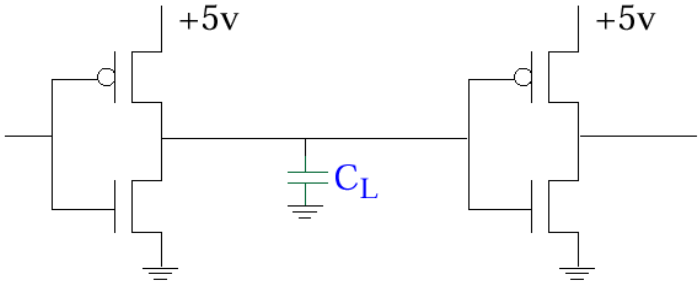
A	Y
0	**1**
1	0





Timing Issues in CMOS

- Recall that it takes time to charge capacitors
- Recall that the gate of a transistor looks like a capacitor
- Wires have resistance and capacitance also!

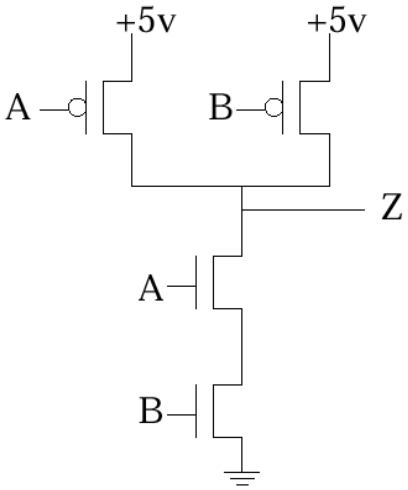


Power Consumption

- Power is consumed in CMOS by charging and discharging capacitors
  - Note that there no static power dissipation in CMOS
  - There's never a DC path to ground
- Good news:
  - You're not consuming power unless you're switching
- Bad news:
  - Switching activity is caused by clock, which is going faster and faster
- If the first-order power effect is capacitor charging/discharging, and the clock causes this:

$$P = C V^2 f$$

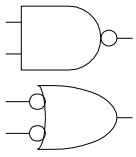
CMOS NAND Gate

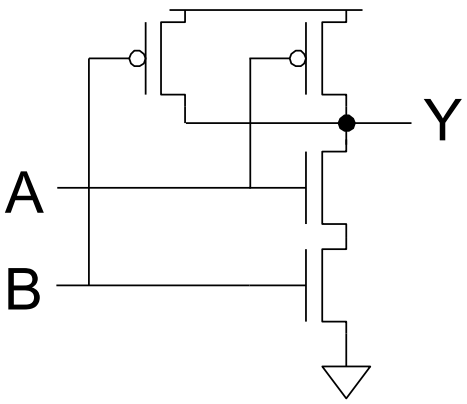


A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND Gate

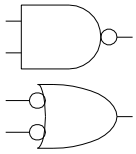
A	B	Y
0	0	
0	1	
1	0	
1	1	

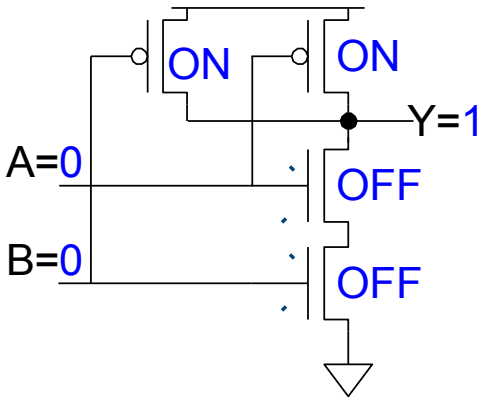




CMOS NAND Gate

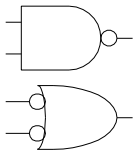
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

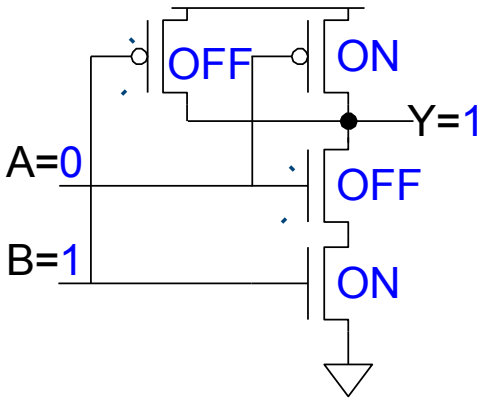




CMOS NAND Gate

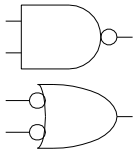
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

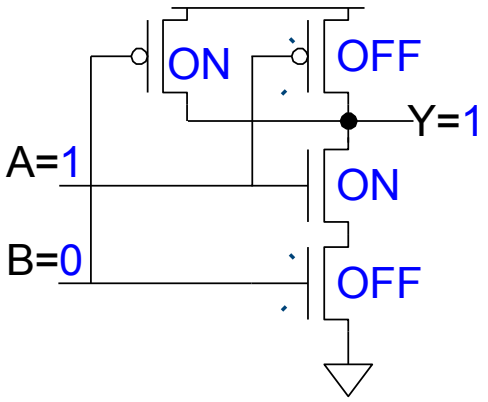




CMOS NAND Gate

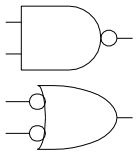
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

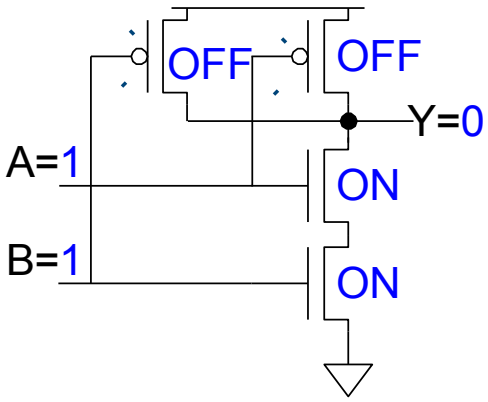




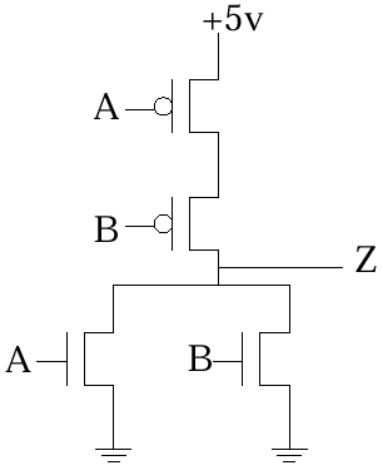
CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

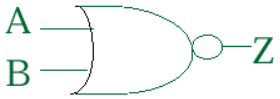




CMOS NOR Gate



A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0



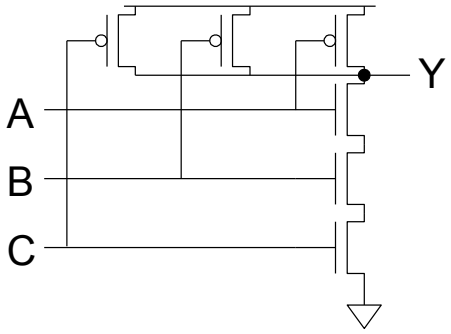
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

Take a moment and draw what you think the transistor circuit for a 3-input NAND gate should be…

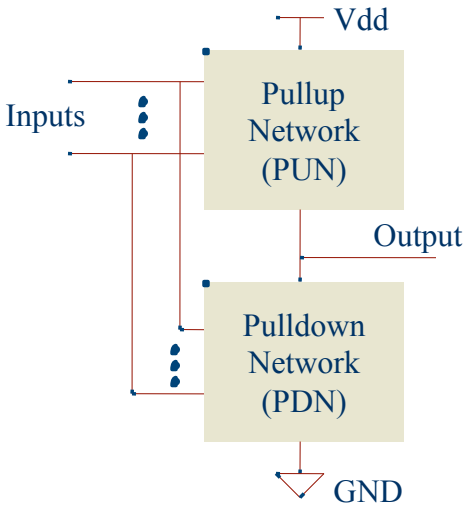
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



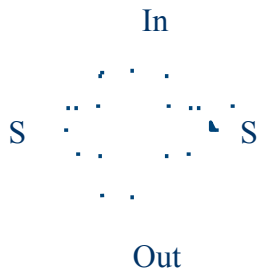
Static CMOS Gate Template

- P-Type pullups and N-Type pulldowns
  - Boolean duals of each other…
  - Note the natural inverting behavior…
    - N-types turn on with high voltages, but pull low
    - P-types turn on with low voltages, but pull high



N-type and P-type Uses

- Because of the imperfect nature of the the transistor switches
  - ALWAYS use N-type to pull low
  - ALWAYS use P-type to pull high
  - If you need to pull both ways, use them both



S=0, In ≠ Out

S=1, In = Out

Switch to Chalkboard

- Complex Gate
- Tri-State
- Latch
- D-register
- XOR